Double Layer Capacitors: Automotive Applications and Modeling

by

David Allen New

B.S.E.E., University of Arkansas (2002)

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Author_____
Department of Electrical Engineering and Computer Science
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Certified by_____
Dr. John G. Kassakian
Professor and Director Laboratory for Electromag. and Elec. Sys.
Thesis Supervisor

Accepted by_____
Arthur C. Smith
Chairman, Department Committee on Graduate Students

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Abstract

This thesis documents the work on the modeling of double layer capacitors (DLCs) and the validation of the modeling procedure. Several experiments were conducted to subject the device under test to a variety of charging/discharging profile and temperatures in an effort to simulate the various conditions such a device might encounter in an automotive type application. High and low current charging profiles were performed for both charge/discharge and charge/hold/discharge type experiments. Low temperature ($\sim -25\,^{\circ}C$), room temperature ($\sim 21\,^{\circ}C$), and high temperature experiments ($\sim 50\,^{\circ}C$) were performed for the investigation of temperature effects on these devices. The derived DLC model was used in PSpice® and Matlab® simulations to determine how accurately the model could predict the performance of the device. The nonlinear characteristics of the device were also investigated and the nonlinear modeling information presented as an addition to the basic DLC model. Device variation was explored for a small sample of these devices in an effort to gain insight on the range of tolerances for modern devices. This work also presents an extensive look into the variety of electrochemical capacitor devices under investigation and in use today. An explanation of these devices and their distributed resistances and capacitance is included. This thesis gives a detailed look into the experimental setups and testing procedures used to test the devices, the simulations for the comparison, and presents the results of the comparison. Finally, this thesis documents the conclusion that this simple model procedure adequately predicts the performance of the device under these various performance profiles.

Thesis Supervisor: Dr. John G. Kassakian
Title: Professor and Director Laboratory for Electromag. and Elec. Sys.

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Contents

List of Figures

List of Tables

Chapter 1

An Overview of Double Layer Capacitor Technologies

1.1 Introduction

Double layer capacitors (DLCs) are an emerging technology that possesses a greater specific energy density (Wh/kg) than conventional capacitors (i.e., electrolytic capacitors) and a higher specific power density (W/kg) than lead-acid automotive battery technologies. Additionally, these devices are light weight, low-volume, and low cost (a predicted cost of ~1¢/F within a few years). Automobile manufactures are interested in the abilities of these devices to enhance existing automotive electrical systems and to make possible the use of new technologies for future automobiles. These new technologies for future automobiles will lead to a more efficient automobile, an increase in safety for the motorist/public, and an improvement in comfort and luxury of the automobile.

The development of equivalent models is a necessary step for using this technology in existing and future systems. This chapter presents a summary of the research completed that contributes to the understanding of these complex devices, the development of equivalent circuit models for these devices, and finally, the investigation of the use of these devices in advanced automotive electrical systems.

1.2 Background Summary

Double layer capacitors go by several names, an example of a few of these names include: ultra-capacitor, super-capacitor, electric double layer capacitor, electrochemical double layer capacitor, and pseudocapacitor. Some recent journal articles seem to attempt to distinguish between the different names according to the dominant storage mechanism (i.e. non-faradaic and faradaic charge storage), while other articles seem to use the different terms interchangeably [1]. The devices investigated during the course of this research program will be referred to in this thesis using the general term—double layer capacitor.

1.2.1 Double Layer Capacitor Basics

Double layer capacitors are an exciting technology that seems to have great potential in both existing and future electronic systems. They have numerous advantages: charge/discharge efficiencies superior to that of batteries, near infinite shelf life and cycleability, minimal (if any) maintenance, and most DLCs can be fully discharged without reducing the lifetime of the device. These capacitors are distinguished from other capacitors in that they are limited to low voltage ratings and have an extremely large capacitance per unit volume as compared to conventional capacitors (sometimes as high as 100 times the capacitance per unit volume of a conventional electrolytic capacitor) [2, 3, 4, 5, 6].

The basic structure of a DLC and some of the more common materials used in the construction of its components can be seen in Fig. 1.1. Double layer capacitors are available currently in both cylindrical (Fig. 1.2) and prismatic packages (Fig. 1.3). An electrically insulating ion permeable separator resides between two activated carbon electrodes. With its near ideal charge/discharge characteristics, carbon is widely used as the electrode material; however, other high surface area materials are also used [7]. Although there is no physical contact between the electrodes, ion transfer does occur [8].

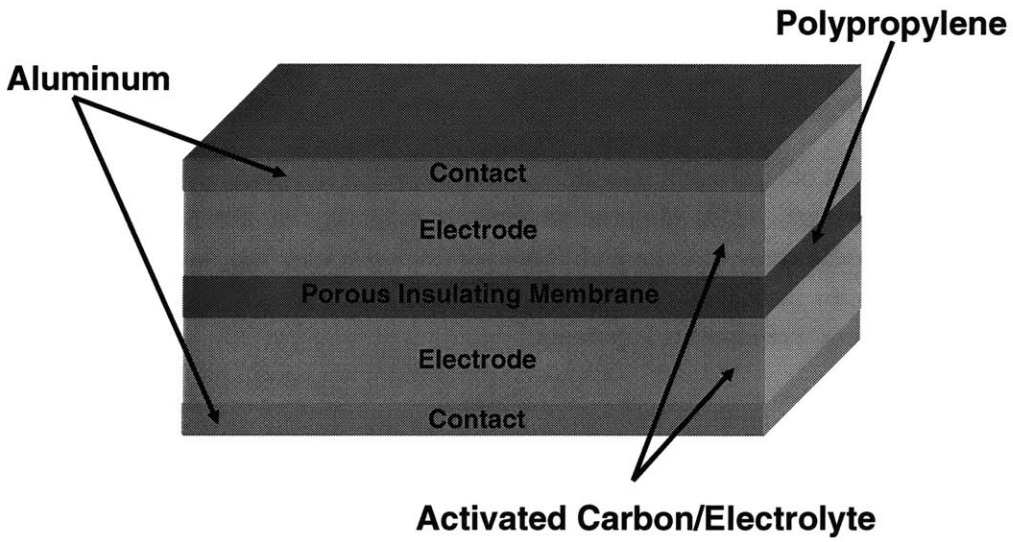

Figure 1.1: Basic Structure of a Double Layer Capacitor

Double layer capacitors can be constructed with either an aqueous or non-aqueous (often an organic) electrolyte. Volumetric energy densities of 5500 Wh/m^3 have been projected when using a DLC with a sulfuric acid electrolyte [9]. In comparison, volumetric energy densities of 20,000 Wh/m^3 have been projected for DLCs that are to be constructed using a non-aqueous electrolyte [9].

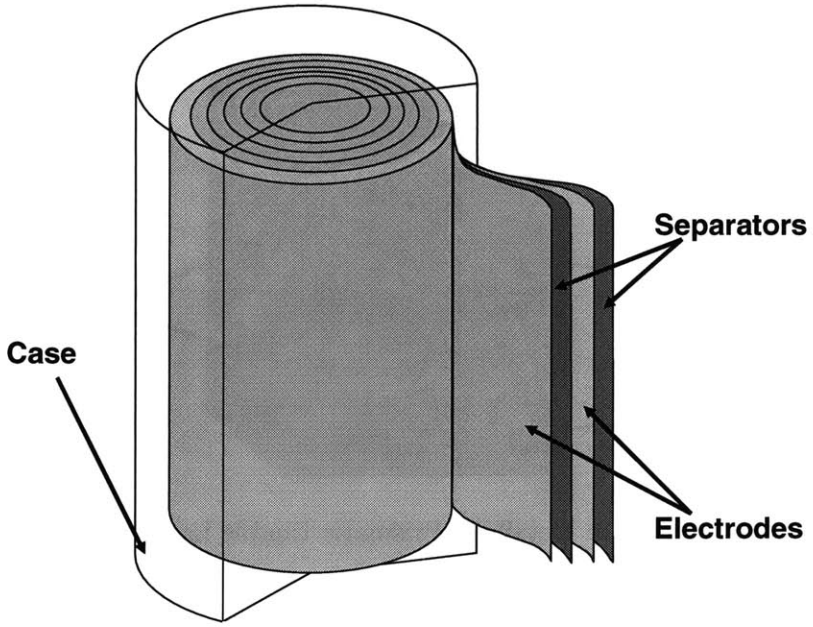

Figure 1.2: Details of Cylindrical Double Layer Capacitor

A relationship between the type of electrolyte used in a DLC and its operating voltage and ESR exist. Aqueous DLCs exhibit a lower ESR and lower operating voltage resulting in lower energy densities and higher power densities than non-aqueous DLCs. In contrast, non-aqueous DLCs exhibit a higher ESR and higher operating voltage which results in a superior energy density but an inferior power density than aqueous based DLC. The DLCs investigated in this research program are devices that use a non-aqueous electrolyte.

1.2.2 DLCs and Conventional Capacitors

An illustration of a conventional capacitor (e.g., an electrolytic capacitor) is shown in Fig. 1.4. The capacitance of this device is given by (1.1) and the distance, d (on the order of 0.01 microns for an electrolytic capacitor [10]), is determined by the thickness of the dielectric used in the device. The area, A, is the surface area of the dielectric film, and $\epsilon_o\epsilon_r$ is the product of the permittivity of free space and the dielectric material used respectively. The capacitance achieved in this device is entirely due to electrostatic charge storage.

$$C = \frac{\epsilon_o \epsilon_r A}{d} \tag{1.1}$$

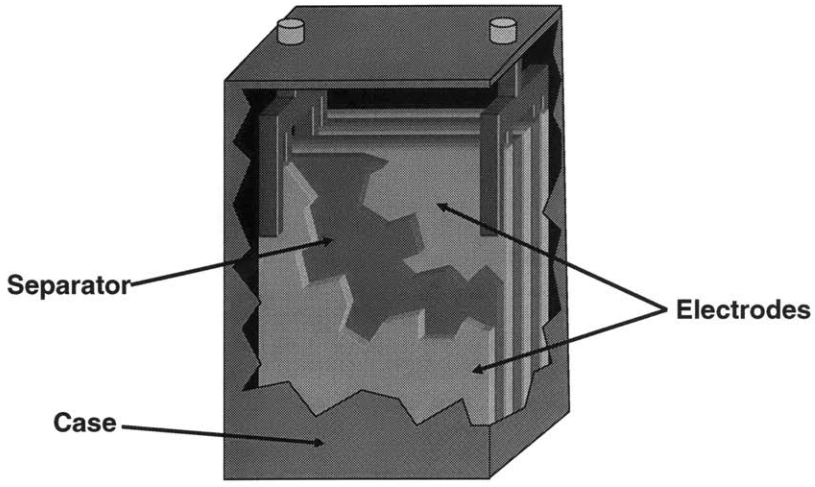

Figure 1.3: Details of Prismatic Double Layer Capacitor

A diagram of a double layer capacitor is provided in Fig. 1.5. The capacitance possessed by a DLC is proportional to surface area, A, of the electrode bulk/electrolyte interface (which is extremely high for a DLC as compared to conventional capacitors—1000-2000 m^2/g for activated carbon) and inversely proportional to the distance, d (on the order of a few angstroms for a DLC), separating the charged ions in the electrolyte from the charges in the electrode bulk material.

Double layer capacitors also store charge electrostatically; however, charge storage occurs at the electric double layer formed at the solid/liquid interface. This phenomena is illustrated in Fig. 1.6). In addition, DLCs can store charge through a faradaic (leading to a capacitance termed "pseudocapacitance") charge storage reaction. The level of pseudocapacitance possessed by the DLC is determined by the materials used for the electrode bulk and electrolyte. This research looks at devices that posses little pseudocapacitance and hence the capacitance of the device is dominated by the relation given in (1.2).

$$C_{DLC} \propto \frac{A}{d} \tag{1.2}$$

1.2.3 Energy Storage Devices

Double layer capacitor technology can be viewed as a hybrid technology somewhere between lead-acid battery technology and conventional electrolytic capacitor technology in that DLCs posses some of the better qualities of the battery device and combine those

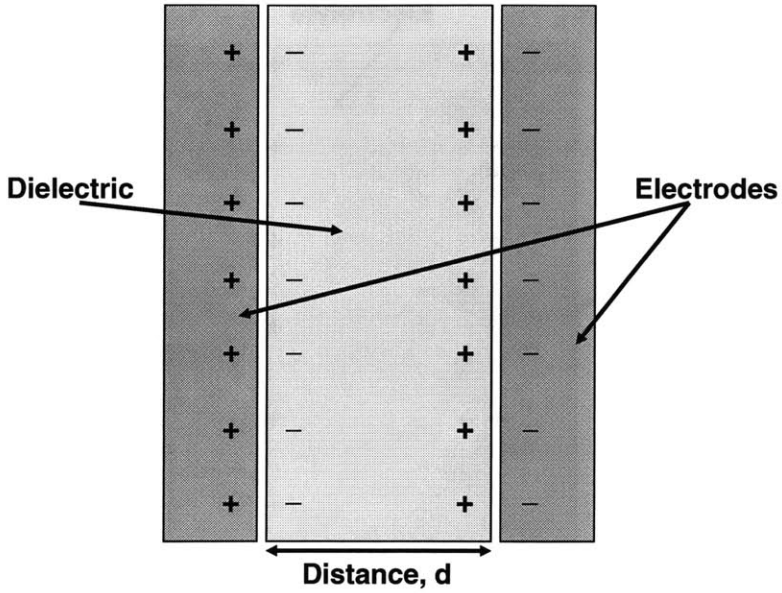

Figure 1.4: Diagram of Conventional Capacitor

qualities with some of the desirable attributes of the electrolytic capacitor. Double layer capacitors can provide high specific (gravimetric) power densities (W/kg), between 10-20 times greater than those of lead-acid battery technologies [1, 11, 12]. They have a higher specific energy density (Wh/kg) than other capacitor technologies. Double layer capacitors energy densities can exceed those of conventional capacitors by approximately 10-100 times [1, 3, 13]. Figure 1.7 shows a Ragone plot of several energy storage technologies. This plot illustrates specific power versus specific energy, where conventional capacitors have the highest specific power rating and battery technology has the highest specific energy rating. Double layer capacitors on this Ragone plot can be seen to bridge the gap between the other two energy storage technologies with respect to specific power and specific energy.

Besides comparing general energy storage technologies, the Ragone plots in Figs. 1.7 & 1.8 also illustrates some of the current DLC technologies available from various DLC manufacturers (Maxwell, 4 devices; NessCap, 6 devices; and Epcos, 13 devices). Fig. 1.8 shows a more detailed look at these commercially available devices. Tables 1.1 - 1.3 tabulate the pertinent data for these 23 devices as shown on manufacture's data sheets. As can be seen in Fig. 1.8, an EPCOS device is plotted with the highest specific power rating of the three manufactures DLC lines shown. A detailed look at the ESR values given for the devices plotted in the Ragone diagram will reveal that the EPCOS line boast the lowest ESR values (as low as 0.2 mΩ). In addition, Fig. 1.8 demonstrates that a NessCap device is plotted as having the highest specific energy of the devices in this plot. NessCap offers the highest rated terminal voltage (2.7 V) of the three DLC lines shown.

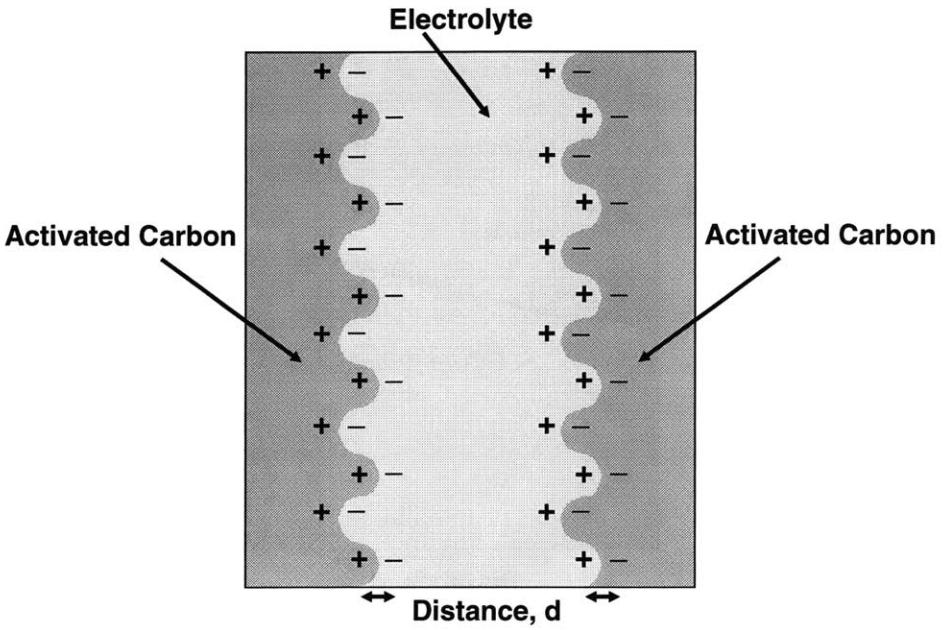

Figure 1.5: Diagram of Double Layer Capacitor

Model	*Maxwell Technologies*				
	Farad	*Continuous Voltage*	*Maximum ESR*	*Specific Power* (W/kg)	*Specific Energy* (Wh/kg)
BCAP0013	450 (-20%/+20%)	2.5 V	2.4 mΩ @ 25°C	3400 @ 2.5 V	2.1 @ 2.5 V
BCAP0014	900 (-20%/+20%)	2.5 V	1.6 mΩ @ 25°C	3800 @ 2.5 V	3.0 @ 2.5 V
BCAP0015	1800 (-20%/+20%)	2.5 V	0.9 mΩ @ 25°C	4300 @ 2.5 V	3.9 @ 2.5 V
BCAP0016	2600 (-20%/+20%)	2.5 V	0.7 mΩ @ 25°C	4300 @ 2.5 V	4.3 @ 2.5 V

Table 1.1: Comparison of Maxwell DLC Technologies

1.2.4 DLCs Contribution to Industry

Recent journal articles and other writings document several applications that may benefit from DLC technology. Many of these applications are sufficiently developed that the DLC may be used to improve efficiency and/or performance by replacing an existing device. Other systems that may benefit from DLC technology are either in the process of being developed now or systems that have been envisioned but are not feasible without the addition of a technology such as the DLC. For instance, the use of DLCs in a system may allow the productions of a portable system that otherwise would require much larger batteries, and therefore would become too bulky to merit production.

The following is a list of existing and conceptual systems that may benefit from the use

Model	*NessCap*				
	Farad	*Continuous Voltage*	*Maximum ESR* (DC 100A)	*Specific Power* (W/kg)†	*Specific Energy* (Wh/kg)†
HP1200P-0023A	1200 (-10%/+30%)	2.3 V	0.7 mΩ	4970	2.32
HP2500P-0023A	2500 (-10%/+30%)	2.3 V	0.5 mΩ	4070	2.83
HP3500P-0023A	3500 (-10%/+30%)	2.3 V	0.4 mΩ	3800	2.96
HP1700P-0027A	1700 (-10%/+30%)	2.7 V	0.7 mΩ	6850	4.53
HP3500P-0027A	3500 (-10%/+30%)	2.7 V	0.5 mΩ	5610	5.45
HP5000P-0027A	5000 (-10%/+30%)	2.7 V	0.4 mΩ	5240	5.82

† Measured at matched load

Table 1.2: Comparison of NessCap DLC Technologies

Model	*EPCOS*				
	Farad	*Continuous Voltage*	*Maximum ESR*	*Specific Power* (W/kg)†	*Specific Energy* (Wh/kg)†
B49300F1605Q000	600 (-10%/+30%)	2.3 V	2.0 mΩ @ 25°C	2300	1.5
B49300G1126Q000	1200 (-10%/+30%)	2.3 V	0.9 mΩ @ 25°C	3700	2.2
B49620A1186Q000	1800 (-10%/+30%)	2.3 V	0.4 mΩ @ 25°C	10700	4.3
B49610A1186Q000	1800 (-10%/+30%)	2.3 V	1.0 mΩ @ 25°C	3800	3.8
B49300G1236Q000	2300 (-10%/+30%)	2.3 V	0.5 mΩ @ 25°C	3600	2.3
B49620A1236Q000	2300 (-10%/+30%)	2.3 V	0.7 mΩ @ 25°C	4800	4.3
B49300L1276Q000	2700 (-10%/+30%)	2.3 V	0.6 mΩ @ 25°C	3000	2.7
B49300A1366Q000	3600 (-10%/+30%)	2.3 V	1.2 mΩ @ 25°C	1700	4.1
B49400A2605Q002	600 (-10%/+30%)	2.5 V	0.6 mΩ @ 25°C	16300	3.3
B49400A2126Q002	1200 (-10%/+30%)	2.5 V	0.4 mΩ @ 25°C	13000	3.5
B49400A2276Q002	2700 (-10%/+30%)	2.5 V	0.23 mΩ @ 25°C	11300	3.9
B49400A2366Q002	3600 (-10%/+30%)	2.5 V	0.2 mΩ @ 25°C	11200	4.5
B49400F2506Q000	5000 (-10%/+30%)	2.5 V	0.25 mΩ @ 25°C	7400	5.1

† Measured at matched load

Table 1.3: Comparison of EPCOS DLC Technologies

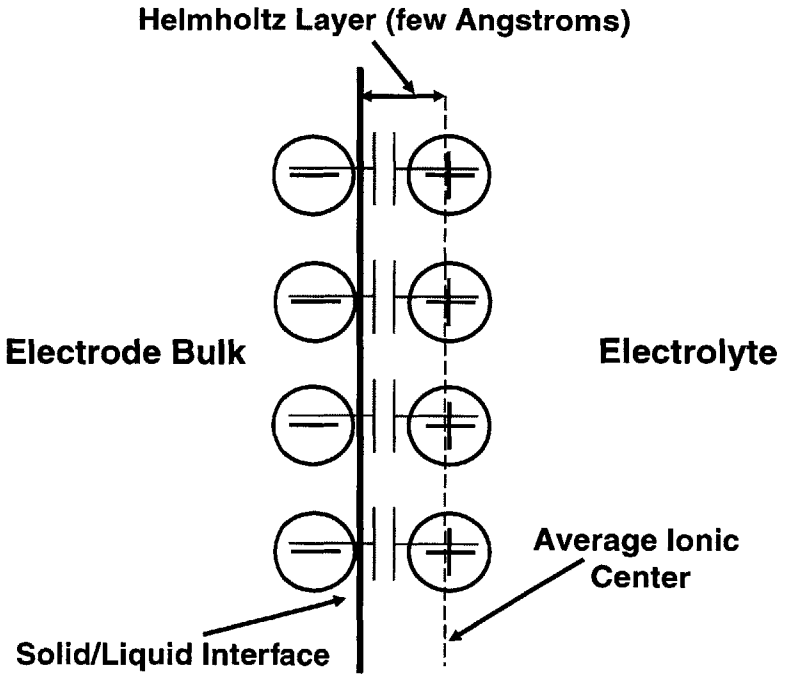

Figure 1.6: Electrode/Electrolyte Interface of a Double Layer Capacitor

of DLC technology: consumer electronics, such as personal digital assistants (PDAs), digital cameras, power tools, toys, digital clocks, wireless communication, GSM-protocol cell phones, two-way pagers, handheld GPS systems, and automotive applications such as automobiles equipped with advanced automotive subsystems, and electric/hybrid cars [12, 14, 15].

This research focuses on DLCs' usability in automotive type applications. These devices are foreseen as devices that may complement a battery in hope of increasing the performance of the system and to improve the system efficiency. Some of the more widely anticipated applications for the DLC may be a brake-by-wire subsystem, a steer-by-wire subsystem, the integrated starter/generator (ISG) and the regenerative braking subsystem. The regenerative braking system could capture energy to charge the DLC, and then this energy may be used to provide peak power for/during acceleration as well as for the starting of the vehicle [7, 13, 16, 17]. Additionally, the DLC may help to load level the battery in an electric/hybrid vehicle (or other system) and to ease peak power requirements for the battery, and to help reduce the chances of the battery suffering from voltage sags and thus, extending the life of the battery [1, 7, 18]. Furthermore, most common batteries are not designed to accept large short bursts of power, as may be required to harness the energy produced in regenerative braking systems, and to do so may damage them [12, 19]. However, DLCs can accept regenerative braking systems' high-pulsed charging energy without

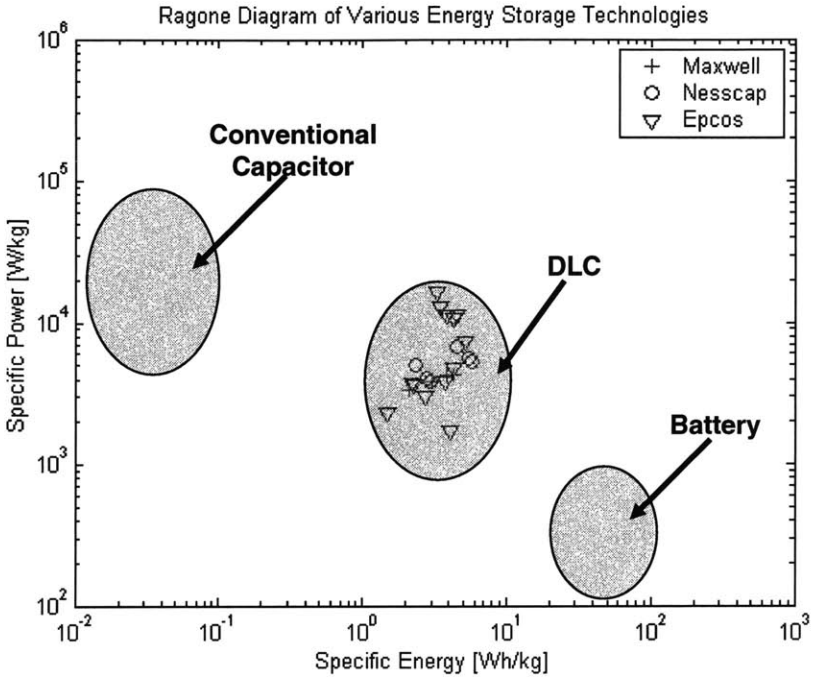

Figure 1.7: Ragone Plot of Various Energy Storage Technologies

negative consequences. Finally, the use of DLCs could allow designers to reduce the number of batteries used in a system and/or reduce the size of batteries used and work towards the elimination of the practice of over-sizing batteries to accommodate peak power demands [1, 12, 20, 21]. This reduction in battery volume and the use of DLCs can lead to a more portable design and improvements in energy management, as well as reductions of system size, weight, and cost [12].

1.2.5 DLC Limitations

The main limitation of DLCs is their low voltage rating (~3 V for non-aqueous based devices). The series combination of the capacitors will increase the voltage of the overall combination of the devices; unfortunately, for the most part, this solution is not enough. Due to manufacturing tolerances, which maybe as high as ±20%, the voltages and energies of each individual capacitor may differ greatly throughout the series-chain of devices, leading to other problems and limiting the lifetime of the devices. This serious issue impedes designing systems such as the 42V PowerNet, which will require the series combination of 17-20 DLCs in order to achieve the needed voltage level [22]. Additional limitations of the DLC include: the capacitance of the DLC may be found to change by up to ±30%

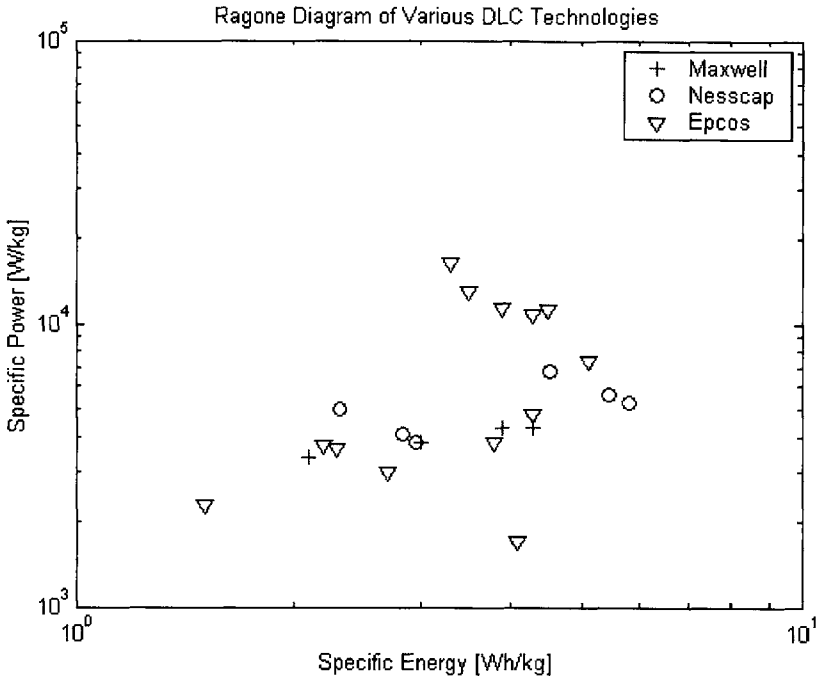

Figure 1.8: Ragone Plot of Various DLC Technologies

depending on the temperature, when pulsed at high charge/discharge rates, they have a reduced capacitance rating, and as with other capacitors, the voltage drops as it discharges thus requiring some from of a voltage regulator in many system designs [1, 23, 24, 25].

Several solutions to the problem of voltage equalization and minimization of device voltage fluctuation have been proposed including the use of: Zener diodes, bleeder resisters, switched resistors, or conventional electrolytic capacitors in parallel, a matrix or array of DLCs (parallel combinations of series-chains in a grid-like formation), dc/dc converters or smart/multi-functional dc/dc converters to raise the voltage level and to regulate an output [16, 22, 26, 27, 28]. Each of the above solutions has its own downside; the use of bleeder resisters and Zener diodes raises concerns of system efficiency; the use of an array of DLCs may be cost prohibitive; and the use of dc/dc converters may be not only cost prohibitive but also create unacceptable system complexity for some designs.

1.2.6 Recent Uses of DLC Technology

Currently, DLCs are being used to supply peak power in some electronic devices, to supply power to IC memories, to provide temporary backup for power systems and electronic

devices, and in the automotive industry [12, 29]. Honda employs DLCs in its new Integrated Motor Assist (IMA) system. In Honda's power assist/power regeneration process, the DLCs provide power to assist in acceleration and store power during braking. Additionally, Honda used DLCs in the J-VX concept car in 1997 and now in their fuel cell powered/regenerative braking equipped FCX.

1.3 Research Summary

After the initial background/literature search on DLCs and their role in automotive type applications, this research focused on the development and validation of simple linear "short-term" DLC models. Furthermore, this research investigated the temperature effects on DLCs, complex non-linear modeling of DLCs, and how DLCs can be used to enhance existing automotive electrical systems and/or future automotive electrical systems.

1.3.1 DLC Model Development

The development of DLC models is a necessary step for exploiting the benefits of this technology. As with many systems, the model can range from very simple to extremely complex, depending on the required level of accuracy that the model is to predict. The use of DLCs as a supplemental energy storage device for advanced automotive electrical systems will require the device to perform under a variety of system profiles from rapid charging/discharging (short-term storage) to long-term storage (e.g., 60 days). Figure 1.9 shows the general form of a "short-term" DLC model. Chapter 3 of this thesis illustrates the development of such a model and Chapters 3 & 4 demonstrated that the DLC can be modeled with acceptable accuracy for short-term charging/discharging as would be required for some advanced automotive electrical systems (e.g., steer by wire, regenerative braking). The procedure used for the extraction of the model parameters for the "short-term" model is similar to the method proposed by Zubieta in his work [30].

A basic diagram of the experimental setup used in the extraction of the DLC model parameters is shown in Fig. 1.10. The test setup illustrated in Fig. 1.10 consists of a HP 6011A power supply operating as a constant current source, the device under test, and a TDS 754D oscilloscope for recording data. For the "Model Extraction" experiment, the device was charged with a constant current (of approximately 100A) to a maximum experimental voltage (approximately 0.5 V) and then open circuited for the remainder of the experiment. Current measurements were taken from the line feeding current into the DLC by a current probe which is fed to the oscilloscope via a current amplifier. Experimental data was then

be dumped into the computer via LabView® so that MATLAB® could be used to filter and plot the data for analysis.

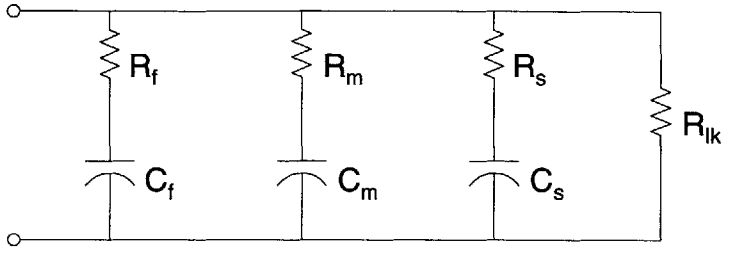

Figure 1.9: General Form of a "Short-term" DLC Model

1.3.2 DLC Model Validation

The DLC behavior is physically complex and the question is raised as to whether a fixed model can be used to describe the device's behavior over a range of conditions. Therefore, in an effort to attempt to validate the model extracted from the "Model Extraction" experiment, the device and model was subjected to a variety of conditions and the results compared. First, the model was subjected to the same testing profile of the "Model Extraction" experiment and the experimental results compared to the simulation results by overlaying the experimental curve with the curve generated by the model. Second, the device (and model) underwent a variety of current profiles that include high and low current charging (discharge via a resistive load) and profiles that investigated the effects that a delay period (between the constant charge and resistive discharge) has on the performance of device. The comparison for the various current profiles include a quantitative investigation of the energy transfer (comparing discharge energy out with charge energy in). The general PSpice® simulation circuit is shown in Fig. 1.11. This figure illustrates the DLC model, a constant current source that generates the pulse of current used to charge the model, the discharge resistance needed when performing simulations that include discharging the device, and the switching network that emulates the switching conditions that the device were subjected to in the lab.

1.3.3 Low/High Temperature Effects

The effect that temperature has on DLCs is important when designing a system that will be subjected to various temperatures (such as in an automotive electrical system). Therefore, this research includes experiments that help explain the effect of temperature on DLCs and

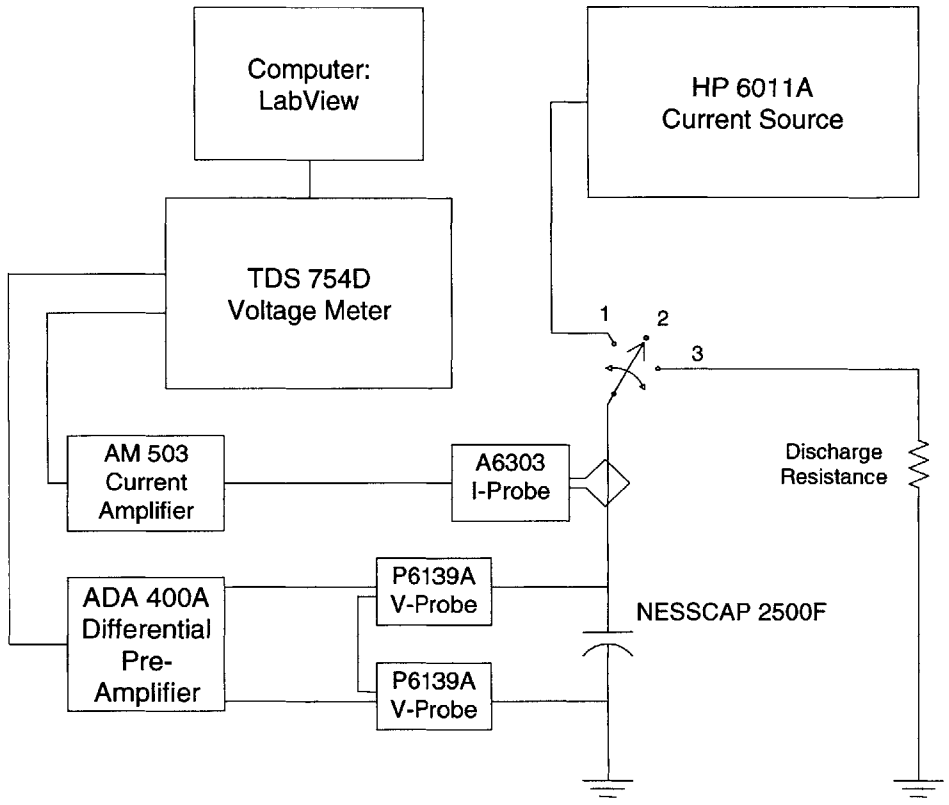

Figure 1.10: Basic Experimental Test Circuit

the models of DLCs. These temperature experiments do not attempt to be as quantitative as the experiments to used when subjecting the device to various current profiles; instead, they are used to determine the trends that temperature has on the model parameters.

For the low-temperature experiment, a low-temperature environment ($-30°C$) cooled the device for a predetermined time period. Next, the device was subjected to a testing profile similar to the one used when extracting the model parameters at room temperature. A low-temperature model was extracted from the low-temperature data to compare to the room temperature model.

In addition to the low-temperature experiment, this research investigated the effect that high-temperature has on DLCs and their models. For the high-temperature experiment, the device was placed in an oven (set at $50°C$) for an extended period of time and then subjected to a testing profile similar to that used when extracting the model parameters at room temperature. The high-temperature data was then used to determine a high-temperature model, which was compared to the room temperature model to determine how elevated temperatures effect DLCs.

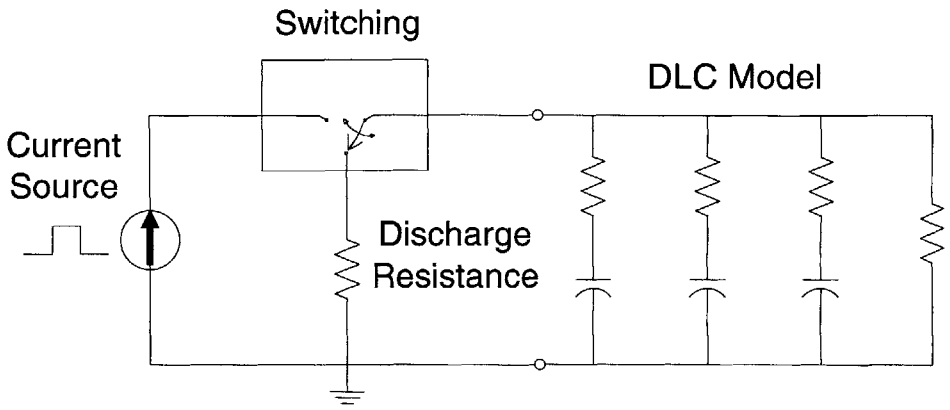

Figure 1.11: Basic PSpice® Simulation Circuit

1.3.4 Non-Linear Capacitances

The non-linear capacitance of the DLCs is a voltage dependent capacitance due to the interfacial tension in the double-layer [30, 31]. The nonlinear capacitance of DLCs, as mentioned in Zubieta's work, is an inherent aspect of DLCs and is therefore an important component of a "complete" DLC model [30]. One goal of this research is to advance the comprehension of this phenomenon. By working towards modeling this aspect of the DLC, this research strives to contribute a better understanding of the non-linear capacitance of DLCs to the field of Electrical Engineering.

Chapter 2

An Introduction to Advanced Electrochemical Energy Storage Devices

2.1 Introduction

Electrochemical energy storage devices, such as batteries, are commonplace in today's consumer products (cell phone, automobiles, personal mobile music devices, laptop computers, television remote controls, etc.). But batteries are not the only form of electrochemical energy storage device available. Electrochemical capacitors are another important form of these devices. Electrochemical capacitors can store charge electrostatically (as a conventional capacitor) or through an oxidation/reduction (redox) process (similar to energy storage by a battery). Table 2.1 gives a comparison of some electrochemical devices and their storage capabilities. The table shows a comparison of three types of electrochemical energy storage devices and the storage capability (given in terms of the number of electrons per atom involved in the storage process). The first device shown is a "general" battery, which relies on an electrochemical reaction as a method of energy storage. The remaining devices shown are electrochemical capacitors (double layer capacitor and pseudocapacitor). The electrochemical capacitor is further classified by two sub-groups, the double layer capacitor (which primary form of energy storage is electrostatic in nature) and the pseudocapacitor (whose primary means of energy storage is via an electrochemical reaction). These sub-groups are distinguished from one another by the device's primary form of energy storage. One important difference to notice between the battery and the two classifications of capacitor technology is that the storage capability of the battery is determined by the bulk material of the electrodes, whereas, for the other two devices, the storage capability primarily depends on the accessible surface area of the electrodes.

Double layer capacitors (DLCs) store charge primarily through an electrostatic mechanism. That is, in the electric field between the conduction band electrons of the electrode material (carbon or metal in some cases) and electrolyte ion accumulation at the double-layer interface. The charge storage is considered a direct or a non-Faradaic form of charge storage (i.e., no intermediate chemical reaction has to occur for the storage of the energy). This form of charge storage is the lowest of the three shown in Table 2.1, but due to the enormous surface

Energy Storage Device Comparison	
Device	*Storage*
Battery	1 - 3 e-/atom of bulk phase material
Double Layer Capacitor	0.17 - 0.20 e-/atom of accessible surface area
Pseudocapacitor	~2.5 e-/atom of accessible surface area†

† Based on ~500 μF/cm2

Table 2.1: Energy Storage Device Comparison [32]

area possessed by these devices, the total amount of energy storage possible is significant. The storage of charge for these devices is on the order of tens of $\mu F/cm^2$ [32, 33].

Pseudocapacitors rely on reduction/oxidation charge storage mechanisms for their primary form of energy storage . This form of charge storage occurs with electron transfer and results in a change in oxidation state of the material involved. During the process of storing charge, the charge is passed through the double-layer (electrode/electrolyte) interface. The electrons involved in this process are valence electrons of the redox material [32, 33].

$$\text{OxidizedMaterial} + \text{e}- \rightleftharpoons \text{ReducedMaterial}$$

The energy storage achievable by indirect or Faradaic charge storage is greater, for a given interfacial area, than that achievable by the double-layer charge storage (however, the indirect method of energy storage is a slower method than the direct method—thus reducing the devices relative power density). Faradaic charge storage is able to achieve values of 100s to 1000s of $\mu F/cm^2$ [32, 33]. The electrode materials used in these devices tend to be transition metal oxides and conducting polymers [34].

In addition to an overview of the many types of electrochemical capacitors and how they store energy, this chapter presents an introduction to several popular electrolytic systems in use for electrochemical energy storage devices. As will be seen, there are several electrolytic systems that are available for electrochemical capacitors and the electrolyte chosen will determine the capabilities of the resulting device. Finally, this chapter concludes with a discussion of the effects of the porous electrode material on the device's behavior and the modeling of that behavior.

2.2 Electrode Discussion

There are several materials to choose from when selecting an electrode bulk material. The choice of material will determine the dominant method of charge storage, and the device's power and energy density capabilities.

2.2.1 Carbonaceous Materials

Carbon electrode based double layer capacitors are one of the most common forms of the DLC available on the market today. The dominant method of charge storage for this electrode material is electrostatic at the electrode bulk/electrolyte interface. This form of capacitance is denoted as a double layer capacitance (C_{dl}), although, depending on the form of carbon used for this electrode, 1 - 5% of the total device capacitance may come from redox charge storage mechanisms (pseudocapacitance, C_{ϕ}) [33].

$$C_{total} = C_{dl} + C_{\phi}$$

Carbonaceous materials are an attractive material for electrochemical energy storage devices. The carbon is available in a variety of porous, high surface area forms, at a reasonably low cost, and its physicochemical properties can be manipulated through various processing (mechanical, thermal, and chemical) techniques. Once processed, the resulting carbon can have good electrical and thermal conductivity, and a high purity. Carbon also has a high resistance to corrosion, which is important when considering energy storage devices that often use a highly corrosive electrolytic solution. Other physical/characteristic features of some forms of carbon which are a product of the processing/treatment method used include: variable pore structure (size, shape), variable pore density, low thermal expansion, and low elasticity [35].

The form of carbon (carbon and carbon composites, which contain one or more metals) to use in electrochemical storage devices is a very important consideration when designing them. A variety of structures such as powder, fibers, thin solid sheet, and bulk carbon are available in addition to the large variety of types of carbons (activated carbon, carbon fibers, aerogels, microbeads, etc.) [32, 35, 36] . Figure 2.1 shows a carbon powder based electrochemical double layer capacitor. In the figure, the powder is shown as circular pellets (in reality, the powder will not be so uniform) that have a large surface area due to the activation process performed on the powder to increase its surface area.

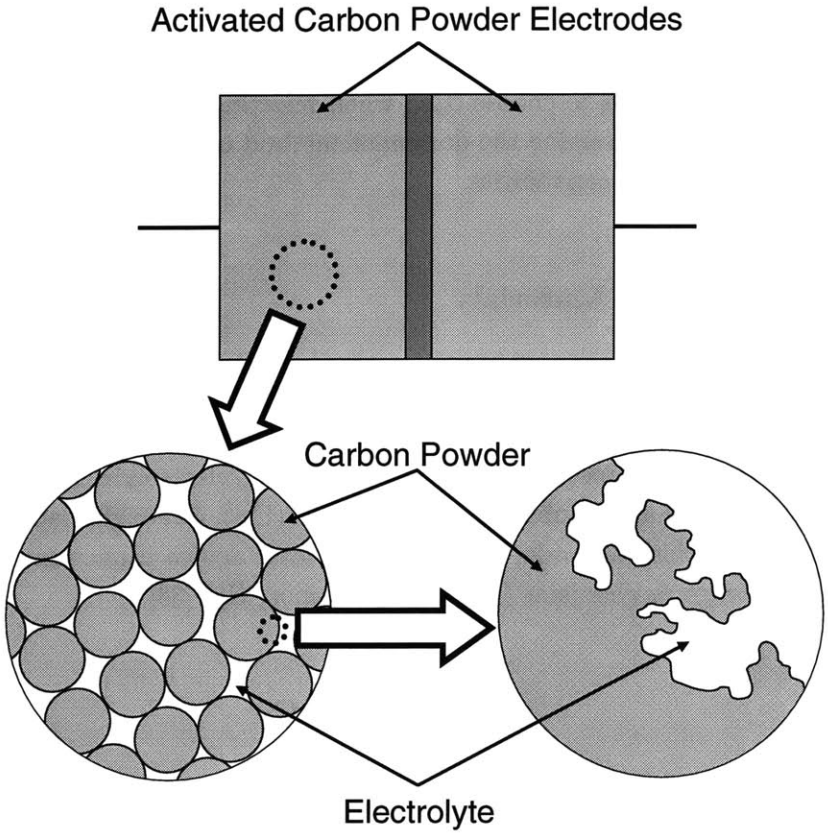

Figure 2.1: Carbon powder electrode DLC

Activated carbon (also known as activated charcoal) is typically a powder or granular structure with a high degree of surface reactivity and a surface area of ~2000 m^2/g. This form of carbon is often made by carbonization (a thermal process which forms tiny pore networks and creates certain functional surface groups) and chemical activation from such precursor material as nutshells (e.g., coconut shells), wood, phenol resin, pitch, and petroleum coke. Table 2.2 gives a comparison of surface area and pore volume for some common precursor materials [32, 36].

This enormous amount of surface area achievable by these materials is due to the extremely porous nature of the processed material. Imagine a granular piece of carbon or a single carbon fiber whose surface is covered in pores (of various sizes), the largest of which are "macropores" (with a diameter of >500 Å) and macropore-channels. Inside the macropores are yet smaller pores (the largest of these are called "mesopores" which measure 20 - 500 Å). The process continues with "micropores" (8 - 20 Å) next, followed by "sub-micropores" (<8 Å). All of these pores contribute to the overall surface area of the material and the material's

Comparison of Raw Carbon Materials		
Raw Material	*Surface Area* (m^2/g)	*Pore Volume* (cm^3/g)
Coconut shell	960 - 2060	0.46 - 1.12
Phenol Resin	2100 - 2350	1.00 - 1.31
Petroleum coke	2600 - 3100	1.39 - 1.78

Table 2.2: Comparison of Raw Carbon Materials [36]

density. "Closed-pores" are pores that are created in the processing of the material that do not effect the overall surface area of the material (as the pores are completely isolated from the outside world; compare to swiss cheese), but do affect the measurable density of the material [35]. An increase in porosity of the processed material results in an increase in overall surface area, but the "effective" surface area only increases to a point. Eventually, the increase in overall surface area is due to the formation of micropores and sub-micropores. The effective surface area of the bulk material is determined by the surface area that the ions in the electrolyte are able to populate. An increased surface area due to pores that are smaller than the ions in the electrolyte does not increase the effective surface area of the material as the ions are not able to take advantage of (populate) this area. The capacitance due to double layer charge storage is typically in the range of 5-10 $\mu F/cm^2$. Given a material with a surface area of 1500 - 2000 m^2/g, the resulting specific capacitance should be approximately 300 - 400 F/g. However, due to the fraction of total surface area that cannot be populated, the resulting specific capacitance (which is dependent on the electrolyte used and the fraction of total surface area due to sub-micropores and micropores; i.e., the electrode's "effective" surface area) is found to be approximately 50 - 150 F/g [34]. The size of the electrolyte ions varies depending on the type of electrolyte used, but typically, the diameter of the ions of an aqueous electrolyte are >20 Å, while the ions of an nonaqueous electrolyte are >50 Å [35]. As electrostatic (non-Faradaic) charge storage is a surface phenomenon, the surface must be accessible to the electrons/ions. The inaccessible bulk material and the closed pores do not contribute to the storage mechanism.

The physicochemical properties (such as surface morphology, porosity of the bulk material, wetability of the surface, and electrical conductivity) of the carbon electrode can be manipulated through complex processing procedures to yield the desired/optimized properties for electrochemical electrodes. These processes include thermal, mechanical, and chemical treatments.

The heat treatment of the electrode is often performed in an inert atmosphere. These processes have the ability to affect the surface area and porosity of the material, and to increase the electrical conductivity of the resulting electrode. The electrical conductivity is increased as the heat treatment decreases the oxygen surface groups by CO and CO_2 formation. Chemical treatment of the material often follows one or two types of heat

treatment. The chemical treatments are used to manipulate the surface area and porosity of the carbon bulk.

The relative number of crystallographic sites (i.e., basal and edge surface sites) greatly determines the electrochemical properties of the processed material. The two types of surface sites include the basal sites and the edge plane sites. The basal sites are relatively inactive electrochemically, whereas, the edge plane site are more reactive. Surface groups (such as –COOH; –OH; –CO; and =O) can form at the edge plane sites and affect the physicochemical properties of the material. An example of these effects include an increase in the number of oxygen surface groups, which results in a lower electrical conductivity, but an improved wetability of the carbon in H_2O (a very important consideration when dealing with aqueous/carbon interfaces, as in aqueous based DLCs) [35].

2.2.1.1 Binders

Many carbon electrodes in use for energy storage devices rely on their construction from carbon powder and fibers. For these systems, a binding material is needed when constructing these devices. Some common binding materials for electrochemical capacitors are polytetrafluoroethylene (PTFE or Teflon®) or phenol-formaldehyde (PF) resin [37].

2.2.2 Metal Oxides

Metal oxide based devices are another form of electrochemical energy storage device. Unlike carbon based device, the primary energy storage mechanism for metal oxide devices is through oxidation/reduction reactions. As with the carbon based device, the total capacitance of the metal oxide device is the sum of the double layer capacitance and the pseudocapacitance.

Some common materials for metal oxide devices are ruthenium oxide (RuO_2), CoO_4, and NiO_2 [34]. Faradaic (redox) charge storage mechanisms provide 5 - 10 times more energy storage capability than double layer (non-Faradaic) energy storage for a give quantity of interfacial surface area, making these devices very appealing. One of the main disadvantages of using these metal oxides as a material in electrochemical devices is cost [33].

In an effort to overcome some of the cost consideration of metal oxide devices and to overcome their shortcomings in terms of surface area (which tends to be lower than many carbon materials), the use of metal oxide/carbon "light" hybrids has been investigated. These hybrids use a high surface area carbon electrode for the substrate, and then deposit (through a

Comparison of Specific Capacitance and Surface Area		
Material	*Specific Capacitance* (F/g)	*Surface Area* (m^2/g)
Carbon	40 - 160	1500 - 2000
Crystalline RuO_2	350	120
Ru (0.4 μm) on C	800	1200†
Ru (0.4 μm) on C	900††	1200†

† Surface area of activated carbon substrate
†† After 100°C heat treatment for 3 hrs.

Table 2.3: Comparison of Specific Capacitance and Surface Area [34, 38]

deposition process such as electroless deposition) the metal oxide (such as ruthenium oxide) onto the carbon [34, 38]. This hybrid then exhibits a higher surface area than the pure metal oxide device, but also relies primarily on redox reactions for its charge storage.

Table 2.3 gives a comparison of three electrode structures. The three configurations include a carbon electrode, a metal oxide electrode (RuO_2), and a "light" hybrid (Ru on C). As can be seen from Table 2.3, the RuO_2 device shows a much higher specific capacitance than the carbon device, even though the surface area of the metal oxide device is an order of magnitude smaller than that of the carbon device. The ruthenium on carbon configuration starts with an activated carbon electrode with a surface area of 1200 m^2/g. The ruthenium is then deposited (0.4 μm) on the carbon. The specific capacitance of this electrode is reported as ~800 F/g. Finally, this hybrid electrode is heat treated for 3 hrs. at 100°C. The reported specific capacitance has increased to ~900 F/g after the thermal treatment [34].

2.2.3 Conducting Polymers

Electrically conducting polymers (ECP) are an interesting material being used by the electronics industry. Some of the motivation behind the implementation of this polymer technology is that the electrical conductivity can be controlled so that the conductivity of the polymer can range from highly-conductive to insulating and that the cost of the materials (the polymer) and the manufacturing of the conducting polymer device has the potential to be low cost (relative to some material currently in use). There are many applications in various fields within the electronics industry (e.g., optoelectronics, energy storage, etc.) for ECPs. Some of these applications include: light emitting diodes (LEDs), laser materials, photovoltaic, photochemical, sensors, electromagnetic interference shielding, and energy storage devices (e.g., solid-state rechargeable batteries and ECP-based/ECP-enhanced supercapacitors) [39].

Summary of Acronyms		
Acronym	*Material*	*Classification*
MPFPT	3-(3,4-difluorophenyl)thiophene	polymer
MPMFPT	3-(3,4,5-trifluorophenyl)thiophene	polymer
Pani	polyaniline	polymer
PCNPT	3-(4-cyanophenyl)thiophene	polymer
pDTT1	poly(dithieno[3,4-b:3′,4′-d]thiophene)	polymer
PFPT	poly[3-(4-fluorophenyl)thiophene]	polymer
pMeT	poly(3-methylthiophene)	polymer
PPy	polypyrrole	polymer
PTh	polythiophene	polymer

Table 2.4: Summary of Acronyms

The field of ECPs is a broad one, even when considering their use as a material in supercapacitors. Several ECPs are being considered (e.g., Pani, pMeT, pDTT1, pFPT, etc.) as an electrode material for supercapacitors, and depending on the ECP used, the ECP may be grown or used as a component of a dry-mix when constructing these electrodes [40]. A table of polymeric materials and their common acronyms are given in Table 2.4. Figures 2.2 - 2.4 show the chemical structure of three types of monomers; pyrrole, aniline, and two thiophene derivatives.

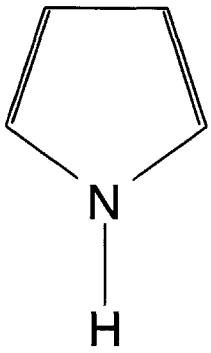

Figure 2.2: Structure of pyrrole [41]

Electrically conducting polymeric devices are similar to the metal oxide devices in that they utilize Faradaic charge storage mechanisms as their primary form of energy storage. The capacitance of an ECP device is due to a double layer capacitance and a redox capacitance [42]. One possible advantage of ECP based devices over metal oxide based devices is the possibility of a lower cost for the ECP electrode material [43]. This however, depends on the choice of ECP; the cost of ECPs varies greatly with the choice of polymer (Pani: ~$120/kg; PTh: ~$22,000/kg) [41].

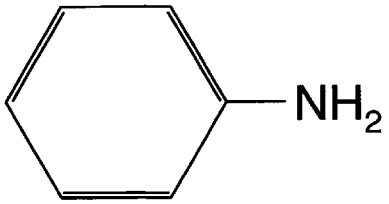

Figure 2.3: Structure of aniline [41]

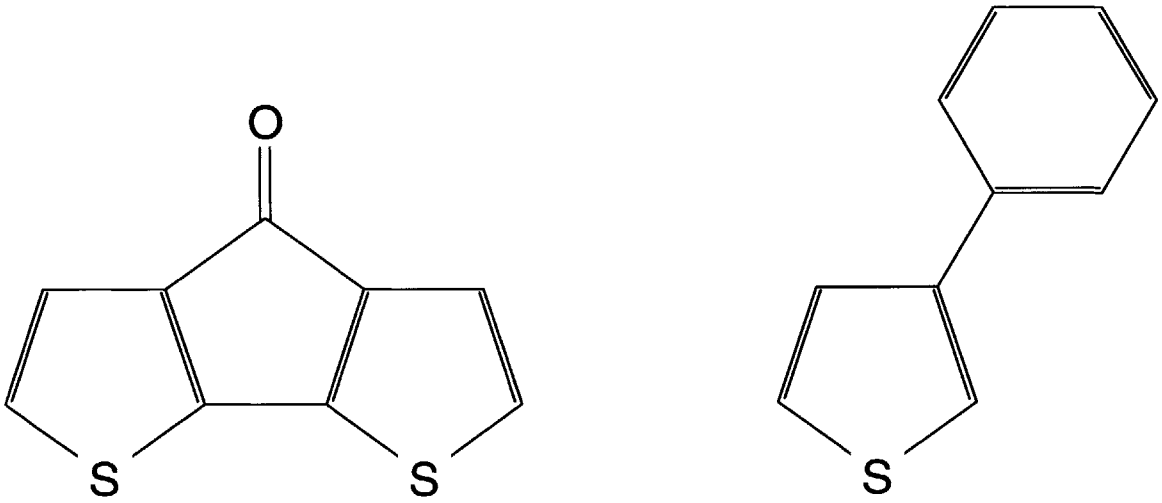

Figure 2.4: Structure of two thiophene derivatives [41]

Conducting polymers for advanced energy storage devices are engineered at the molecular level, which allows the manipulation of their electrochemical/physicochemical properties. Additionally, they may be processed easily into thin-films, or molded into a variety of shapes. The polymer used for these devices need the ability to be heavily doped (p-doped or n-doped) and provide good reversibility when charging and discharging [44].

Polymers that are n-doped, tend to have poor electrochemical stability and have lower doping levels than polymers that are p-doped. The doping level of these materials is on the order of ~0.10 electrons per monomer unit (e/mu). While, p-doped polymers often have doping levels on the order of 0.25 - 0.33 e/mu and show good levels of reversibility [44].

2.2.3.1 Types of ECP Devices

There are three types, or classifications, of polymeric supercapacitors (Type 1, Type 2, and Type 3). Type 1 devices use the same dopable material for both the cathode and anode of the device. Type 2 devices will use two different polymers for the two electrodes. And, Type 3 devices use the same polymer for both electrodes, however, in a different manner than Type 1 devices [41].

Some examples of Type 1 devices are Pani-Pani, PTh-PTh, or PPy-PPy. For these devices, when the device is fully charged, one electrode is fully doped (usually p-doped as the p-doped polymers tend to be superior to there n-doped counterparts for energy storage devices) while the other is undoped. When the device begins to discharge, the fully doped electrode begins to de-dope while the undoped electrode begins to become doped. At the point that the device is discharged (i.e., the device's voltage is $\sim$0 V) both electrodes are approximately half doped. The cell voltage for this type of device is typically 1 - 1.2 V [41, 45].

For Type 2 devices, two different polymers are used for the two electrodes. Even though two types of polymers are used, both electrode materials will be either p-dopable or n-dopable. The charging/discharging (doping/de-doping) process for the Type 2 device is similar to the processes of the Type 1 device. When the device is fully charged, one electrode is fully doped (either n- or p-doped) while the other is undoped. When the device begins to discharge, the fully doped electrode begins to de-dope while the undoped electrode begins to become doped. At the point that the device is discharged (i.e., the device's voltage is $\sim$0 V) both electrodes are approximately half doped. A few examples of Type 2 polymer combinations include PPy-PANI or PPy-PTh. Type 2 devices typically have a cell voltage up to $\sim$1.5 V [41, 45].

The final classification of ECP devices is the Type 3 device. The Type 3 device uses the same polymeric material for both its anode and cathode (as the Type 1 configuration does). However, in the Type 3 configuration, one electrode is n-dopable, while the other is p-dopable. During charging of the Type 3 device, the electrode to be p-doped gives up an electron from the polymer backbone (through the external circuit) while an anion from the electrolyte is given to the polymer to maintain charge neutrality. The electrode to be n-doped takes an electron during charging while a cation is received by the polymer. When the device is charged, one electrode is n-doped while the other is p-doped. When the device begins to discharge, both electrodes begin to de-dope. Once the device is discharged, both electrodes return to their undoped state. The cell voltage of Type 3 devices can be $\sim$3 V. An example of a material used for Type 3 devices in PTh [41, 43, 45, 46].

Some advantages of Type 3 devices over the Type 1 & 2 devices include: I) The possible potential range of the device is greater, which leads to higher device energy densities. II) Type 1 and Type 2 devices when charged have one electrode undoped. The undoped electrode is in the semi-insulating state, which leads to a lower power density. For Type 3 devices, both electrodes are doped when the device is charged. The polymer tends to have a much lower resistance in the doped state, which leads to higher power densities possible if both electrodes are doped (due to the higher conductivity of the electrode material). III) The voltage profile can remain (depending on the device configuration) approximately constant (rather than dropping linearly with discharge) during discharge. This allows most of the charge stored in the device to be used at the higher voltage levels (like a battery) and is helpful when designing systems involving these devices [43, 45].

2.2.3.2 Pani based ECP Supercapacitors

There are several properties possessed by the Pani material that suggest that it would be a suitable electrode material for supercapacitors. Polyaniline possesses high environmental stability, it is easy to process, and the electrical conductivity is controllable. In order to use Pani as a material for supercapacitor electrodes, the Pani must be doped with a compound such as a lithium-ion salt (Pani-$LiPF_6$). The choice of electrolyte used in the supercapacitor is as important as the choice of electrode material used and the two materials must be matched. A suitable electrolyte used with Pani-$LiPF_6$ electrode is tetraethylammonium tetrafluoroborate (Et_4NBF_4) in acetonitrile [47].

The construction of a basic Pani-based supercapacitor is illustrated in Fig. 2.5. The cell consist of two Pani electrodes (50% Pani, 40% carbon black as a conducting agent, 10% binding material) separated by a PTFE (Teflon®) separator that is electrically insulating and ionically conducting and a pair of aluminum current collectors. The five layers are sandwiched together and wrapped in filter paper before being placed in a Teflon® casing filled with Et_4NBF_4 and acetonitrile.

A majority of the supercapacitor devices available on the market today are carbon-based devices. Conducting polymers as a material for supercapacitors has received so much attention recently since the cost of the ECP material and the manufacturing of that material is expected to be less than that of the activated carbon and that the ECP supercapacitor has been shown to outperform the carbon-based supercapacitor in terms of specific energy and specific power. One figure of merit that is used to compare and judge supercapacitors is their specific discharge capacitance (F/g). Figure 2.6 shows the performance of two supercapacitors (carbon and Pani-$LiPF_6$) in terms of discharge capacitance versus the number of

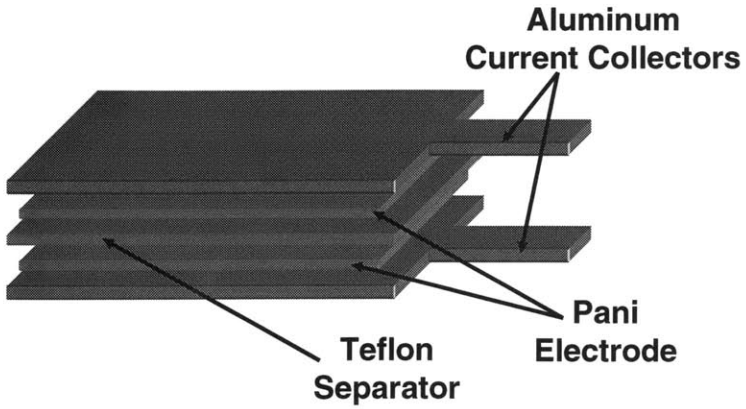

Figure 2.5: Basic Construction of a Pani-based Supercapacitor [47]

cycles. As can be seen in this figure, the carbon-based device (constructed similarly to the Pani device illustrated in Fig. 2.5, with a 90% carbon and 10% binding material ratio) is seen to have a nearly constant discharge capacitance of ~1.9 F/g over the range of 0 to 1000 cycles. On the other hand, the discharge capacitance of the Pani-$LiPF_6$ device is seen to be much higher than the carbon-based device and that it decreases in a nearly linear fashion from ~107 F/g to ~84 F/g over the range of 0 to 10,000 cycles [47]. An important note to consider when comparing these two performance curves is that a plot of the discharge capacitance for the Pani-$LiPF_6$ device over the range of 0 to 1000 cycles will a appear as a nearly constant discharge capacitance (assuming the linear rate of change as seen in Fig. 2.6). In conclusion, in terms of discharge capacitance, it is shown that the addition of the polymer to the basic carbon electrode device, can greatly improve the device's performance.

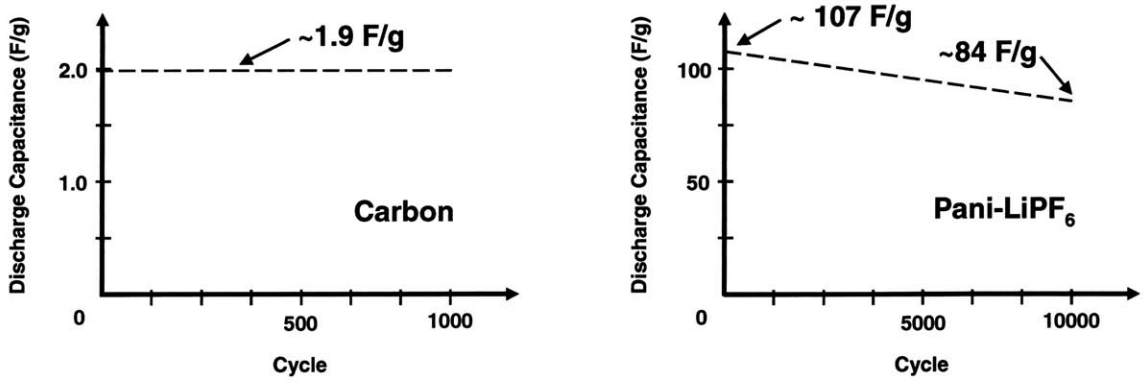

Figure 2.6: Discharge Capacitance versus Number of Cycles [47]

2.2.3.3 pMeT based ECP Supercapacitors

Poly(3-methylthiophene) is another polymer that is actively being pursued as an electrode material for supercapacitors. An advantage of this polymer is that it can either be deposited on an electrode by monomer oxidation or it may be formed into an electrode by performing a dry-mix of pMeT, a conducting additive (carbon), and a binder (carboxy methyl cellulose) [40]. As can be seen in Fig. 2.7, the discharge capacitance of the pMeT electrode material has been found to be ~240 F/g over the range of 0 to 1000 cycles which in terms of discharge capacitance, outperforms both the carbon-based device and the Pani device illustrated in Fig. 2.6.

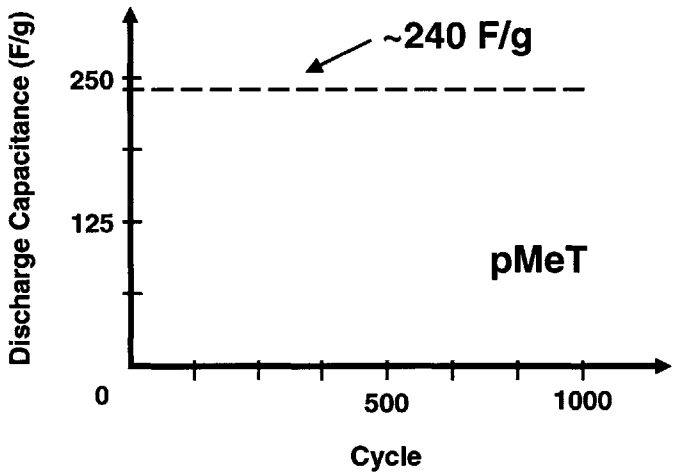

Figure 2.7: Discharge Capacitance versus Number of Cycles [48]

2.2.4 Hybrid Devices

A hybrid device is a device that utilizes more than one of the three advanced electrochemical capacitor technologies. This hybrid device can be constructed as an ECP/carbon hybrid (i.e., with one ECP electrode and one carbon electrode) or a metal oxide/carbon hybrid (i.e., with one metal oxide electrode and one carbon electrode). Another "light" hybrid is one that uses a carbon electrode as a high surface area substrate for the deposition of a redox material (ECP or metal oxide). These light hybrids take advantage of the high surface area material and the large energy storage capabilities of the redox material. This subsection gives an example of a ECP/carbon hybrid.

The performance of an n/p ECP supercapacitor (i.e., one that uses the same polymer material for both the n-electrode and p-electrode) is sometimes limited by the "weaker" of

n/p pMeT	*p-electrode*	*n-electrode*
Capacitance (F/g)	240	180
Capacity (mAh/g)	70	30
Resistance	low($\sim$2 Ωcm^2)	very high

Table 2.5: n/p pMeT Supercapacitor [40, 49]

Material	*p-electrode*	*n-electrode*
AC1	74 F/g	84 F/g
AC3	125 F/g	158 F/g

Table 2.6: Capacitance of Activated Carbon [40]

the two electrode. Such is the case for n/p pMeT supercapacitors. Several parameters as they pertain to n/p pMeT supercapacitors are illustrated in Table 2.5. The information in Table 2.5 shows that in terms of specific capacitance, capacity, and resistance, the n-electrode of the n/p pMeT supercapacitor is inferior to that of the p-electrode. The 180 F/g capacitance value of the p-electrode is still a high capacitance value and not the main concern in regards to using pMeT for the p-electrode. However, the low capacity (less than half of that found in the p-electrode), and the very high resistance is the limiting factor in using pMeT for the n-electrode in a supercapacitor [40].

Given the characteristics of the pMeT p-electrode shown in Table 2.5, it is still desirable to use pMeT as a supercapacitor material, assuming a suitable n-electrode material can be found. Table 2.6 illustrates the specific capacitance values of two activated carbon materials (AC1 and AC3). As can be seen from this table, the n-electrode is the superior of the two (for both AC1 and AC3). Additionally, we know activated carbon to have an acceptable value of capacity for supercapacitor electrodes and a low value of resistance (with the n-electrode resistance being the lower of the pair).

Using pMeT for the p-electrode and activated carbon for the n-electrode results in the construction of a hybrid supercapacitor that takes advantage of the strong qualities of both materials. Figure 2.8 compares the performance of an activated carbon-based supercapacitor and a hybrid supercapacitor that uses an activated carbon n-electrode and pMeT p-electrode. As can be seen from this figure, the hybrid device outperforms the carbon device in terms of specific power and specific energy [40, 49].

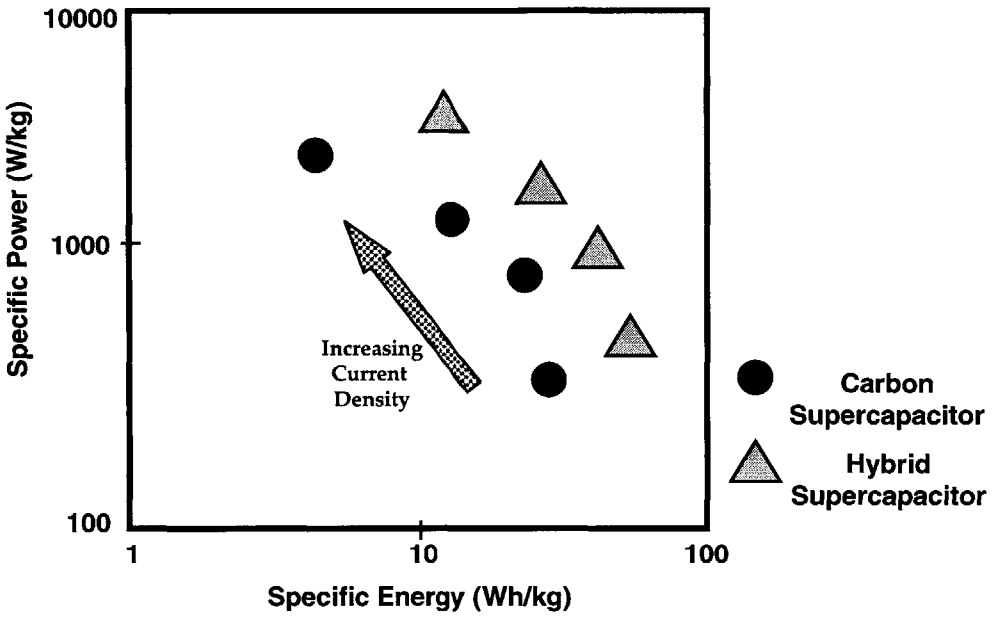

Figure 2.8: Comparison of Carbon-based and Hybrid Supercapacitor [40, 49]

2.3 Electrolyte Discussion

The electrolyte of the electrochemical energy storage device is another component of the device that further classifies it into yet another category. Already mentioned was the distinction between different types of electrochemical capacitors: namely DLCs and pseudo-capacitors. Now the distinction among these devices becomes a little more specific based on the electrolyte used in the system. There are several classifications of electrolytes for electrochemical energy storage devices. These include aqueous, nonaqueous (organic), polymeric, and molten salts. All of these systems have their advantages/disadvantages. Electrochemical electrolytes (composed of a solute and a solvent) need to posses high electrolytic conductivity, thermal stability, electrochemical stability, the ability to posses a high salt (solute) concentration, and to do so over a wide range of temperatures [32, 36, 50].

2.3.1 Aqueous Electrolyte

Aqueous electrolytes are solutions comprised of an electrolytic salt (solute) in an aqueous solvent. An example of some aqueous electrolytes currently employed in electrochemical devices include: sulfuric acid (H_2SO_4), potassium hydroxide (KOH), and sodium hydroxide (NaOH). The electrolytes used in these systems tend to be somewhat corrosive, especially at high concentrations. For this reason, many designers choose to use bases over concen-

trated acids. A balance must be achieved among the electrolyte used, its concentration, the electrode material used, and the design requirements (ESR, power density, etc.).

Aqueous electrolytes are attractive for electrochemical devices for several reasons. 1) The concentration of the electrolyte is easily controllable and high concentrations are possible. The high concentration of the electrolyte can result in a minimization of the devices ESR and lead to higher power densities. 2) The cost of the aqueous electrolyte is less than the organic electrolytes. 3) The ions of the aqueous electrolyte are often smaller than those of the nonaqueous solution, which can result in the population of smaller pores than is possible with other solutions, resulting is greater energy storage and device energy density measurements. 4) An aqueous based device may have the ability to be serviced/maintained as one would treat many lead-acid batteries, rather than replacing the device should the quantity of electrolyte or its concentration change over the course of its lifetime. One main disadvantage for some systems that would benefit from electrochemical capacitors is the low voltage level of aqueous based systems. The maximum cell voltage of an aqueous based electrochemical capacitor is ~1.2 V.

2.3.2 Nonaqueous Electrolyte

Nonaqueous electrolytes are composed of a solute (electrolytic salt) and a solvent (or mixture of solvents). An example of some common salts are tetraethylammonium hexafluorophosphate (Et_4NPF_6) and tetraethylmethylammonium hexafluorophosphate (Et_3MeNPF_6). An example of some common solvents are acetonitrile (AN), and propylene carbonate (PC) [32]. Table 2.7 gives a summary of many electrolyte components used in electrochemical nonaqueous capacitors. There are three main classifications of nonaqueous electrolyte systems; high, intermediate, and low dielectric constants. An example of high dielectric constant aprotic solvents are ethylene carbonate, and PC. Some intermediate dielectric constant aprotic solvents include AN, dimethylacetamide, and butyrolactone, while low dielectric constant solvents include dimethoxyethane and tetrahydrofuran [32].

Compared to many aqueous electrolytes, the nonaqueous systems tend to be more costly. The processing of these solutions is very complicated as the product must have a very high level of purity. The produced salts must be very dry and the resulting solution must be free of water. The poor processing of these electrolytic systems can lead to H_2 and O_2 formation during device discharge which can result in a reduction in lifetime and poor discharge characteristics of the device. The formation of H_2 and O_2 gases are able to occur in these devices as the voltage of these devices is greater than the decomposition voltage of aqueous solutions. With the appropriate choice of electrolyte materials, the operating voltage of the device can reach 3 - 4 V [32].

Summary of Acronyms		
Acronym	*Material*	*Classification*
AN (CH_3CN)	acetonitrile	solvent
BL	butyrolactone	solvent
DMA	dimethylacetamide	solvent
DMC	dimethyl carbonate	solvent
DME	dimethoxyethane	solvent
DMF	dimethylformamide	solvent
EC	ethylene carbonate	solvent
EtOH	ethanol	solvent
TEA	tetraethylammonium	salt
TEATFB (Et_4NBF_4)	tetraethylammonium tetrafluoroborate	salt
Et_4NPF_6	tetraethylammonium hexafluorophosphate	salt
Et_3MeNPF_6	tetraethylmethylammonium hexafluorophosphate	salt
$LiClO_4$	lithium perchlorate	salt
PAN (C_3H_3N)	poly(acrylonitrile)	solute (polymeric)
PC	propylene carbonate	solvent
TAA	tetraalkylammonium	salt
THF	tetrahydrofuran	solvent
M_5IIm	pentamethyl imidazolium bis(trifluoromethylsulfonyl)imide	salt (imidazolium)
M_5IPF_6	pentamethyl imidazolium hexafluorophosphate	salt (imidazolium)
TMAOTf ($Me_4NCF_3SO_3$)	tetramethylammonium trifluoromethanesulfonate	salt
TBAIm	tetrabutylammonium bistrifluoromethanesulfonimide	salt
TEAIm	tetraethylammonium bistrifluoromethanesulfonimide	salt
DMEIIm	dimethylethylimidazolium bistrifluoromethanesulfonimide	ionic liquid
DMPIIm	dimethylpropylimidazolium bistrifluoromethanesulfonimide	ionic liquid

Table 2.7: Summary of Acronyms

Besides processing requirements, there are several additional requirements for nonaqueous solutions used in electrochemical devices. 1) The electrolyte chosen should be aprotic, that is, the electrolyte should be incapable of acting as a proton donor at its working voltage. Failure to adhere to this requirement can result in the formation of H_2 at the cathode of the charged device. Again this will reduce the lifetime of the device and/or result in a reduction in device performance. 2) The voltage window (range of voltage) of the solution needs to be greater than the range of voltages in which the device is to be used in order to reduce the chances of over-voltaging the device which will result in solution (usually salt) decomposition. 3) The solution's ionic viscosity should be as low as possible in order to maximize the mobility of the ions. The device's ESR and power density are directly related to the ionic mobility of the solution [32]. 4) The chosen salt (solute) must have good solubility for the chosen solvent. Poor solubility will result in low salt concentrations, lower power densities, and a higher ESR. A high salt concentration will lead to low ohmic resistances, low polarization, whereas a low salt concentration will limit the achievable energy density of the device as the salt will be the limiting factor in the charge storage capability of the device. Too low of a salt concentration will result in poor population of the interfacial surface, leading to a reduction in stored charge, and finally a lower than optimum device energy density [32, 50].

2.3.3 Polymeric Electrolyte

Polymeric solid electrolytes are another form of electrolytes available for electrochemical devices. The main advantages of these electrochemical systems are that the devices are highly reliable in terms of the elimination of electrolyte leakage, and that high energy densities are possible due to the high possible voltages of the device (~5 V). However, there are some disadvantages and difficulties with regard to these devices. There is a low solubility of the salt in the polymer matrix, low conductivity of the material at room temperature, and poor electrical contact at the electrode bulk/electrolyte interface; all leading to a device with a high ESR [51].

2.3.4 Conclusion

As can be seen from the above discussion, there are a variety of electrolyte systems to choose from when designing an electrochemical capacitor. Some of the main design considerations are cost, ESR, power density, energy density, complexity of production, and the device's operating voltage.

Table 2.8 gives a comparison of three different electrolyte classifications (aqueous, nonaque-

Comparison of Electrolyte Classifications and Conductivity		
Electrolyte Classification	*Salt and Solvent*	*Conductivity* (mS/cm)
Aqueous	HCl/H_2O	849
Aqueous	$MgCl_2/H_2O$	160.3
Nonaqueous	$MgCl_2$/EtOH	23.0
Nonaqueous	$LiClO_4$/PC/DME	14.38
Nonaqueous	Et_4NBF_4/PC/DME	13
Nonaqueous	M_5IIm/PC	10
Nonaqueous	M_5IPF_6/PC	9.9
Nonaqueous	$LiClO_4$/PC	5.420
Polymer	EC/PC/$LiClO_4$/PAN	1.7

Table 2.8: Comparison of Electrolyte Classifications and Conductivity [32, 52]

ous, and polymeric), several electrolyte systems, and their conductivity. As can be seen from this summary, the aqueous systems provide the highest conductivity; the polymeric show the lowest, while the nonaqueous systems fall in between.

2.4 Distributed Resistances and Capacitances

As seen in Figs. 2.9 & 2.10, a capacitance is created at the interface of the electrode bulk material and the electrolyte once the ionic charges in the bulk material and the electrolyte accumulate at the interface surface. An increase in the surface area of the interface will allow the possibility of an increase in capacitance (assuming a sufficient ion population, mobility, pore wetting, and ion-pore matching), as the capacitance is directly proportional to the effective surface area. With carbon-based DLCs, the material is typically a porous activated carbon powder with a specific surface area on the order of a few thousands of m^2/g. But due to the finite mobility of the ions and the fact that the surface is of a porous nature, one with varying sizes of pores (macropores, mesopores, micropores, and sub-micropores; see Fig. 2.11), the ions are not able to sufficiently charge the entire surface area of the device at all frequencies. At the lower frequencies (approaching dc), the ions have sufficient time to move into the smaller pores. As the frequency is increased, the ions do not have sufficient time to totally charge these smaller pores, and may only charge the larger macropores. The difference in capacitance of the device in the lower and higher frequency regimes is significant; the effective surface area in the higher frequency case is largely due to the surface area of the macropores, whereas, in the lower frequency cases, assuming the frequency is low enough (sufficient time allowed) and ion mobility and population do not hinder the process, the effective surface area of the device includes not only the surface area due to the macropores, but also that of the mesopores, and micropores (assuming

ion-pore size matching) and hence the ions populating these smaller pores greatly increase the effective surface area of the interface and the capacitance of the device.

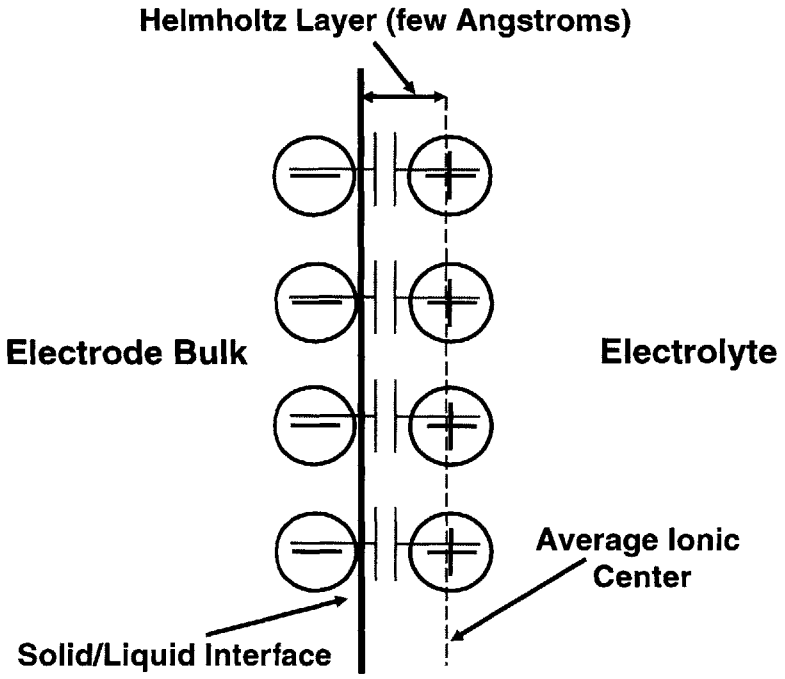

Figure 2.9: Electrode/Electrolyte Interface of a Double Layer Capacitor

This changing of surface area (and hence capacitance) with frequency as the pores "tune" in or out does not allow the use of a simple RLC model when modeling DLCs, but in fact has led researchers to use a distributed resistance and capacitance model for these devices. The distributed capacitance is due to the process outlined above, but the distributed resistance may not be so intuitive. In order to understand the distributed resistance inherent in these devices, one must first explore the resistances the ions encounter during their charging and discharging process. As shown in Fig. 2.10, there are ions present in both the electrolyte and the bulk (carbon) material. The ions in the electrolyte encounter a resistance when attempting to pass through the ion-permeable membrane, a resistance when traversing the electrolyte, and a form of resistance when attempting to populate the pores. The ions found in the bulk material encounter a "path" resistance due to the ions traveling through the collector and carbon materials as well as "contact" resistances between the collector and carbon material and between the pellets of activated carbon powder bulk material. The "path" and "contact" resistances of the ions populating the bulk material are significantly smaller (due to the nature of the material used, the small lengths involved, and the packaging processes) than the resistances encountered by the electrolyte ions and hence are ignored in many formulations of DLC models. It is primarily the resistances encountered by the

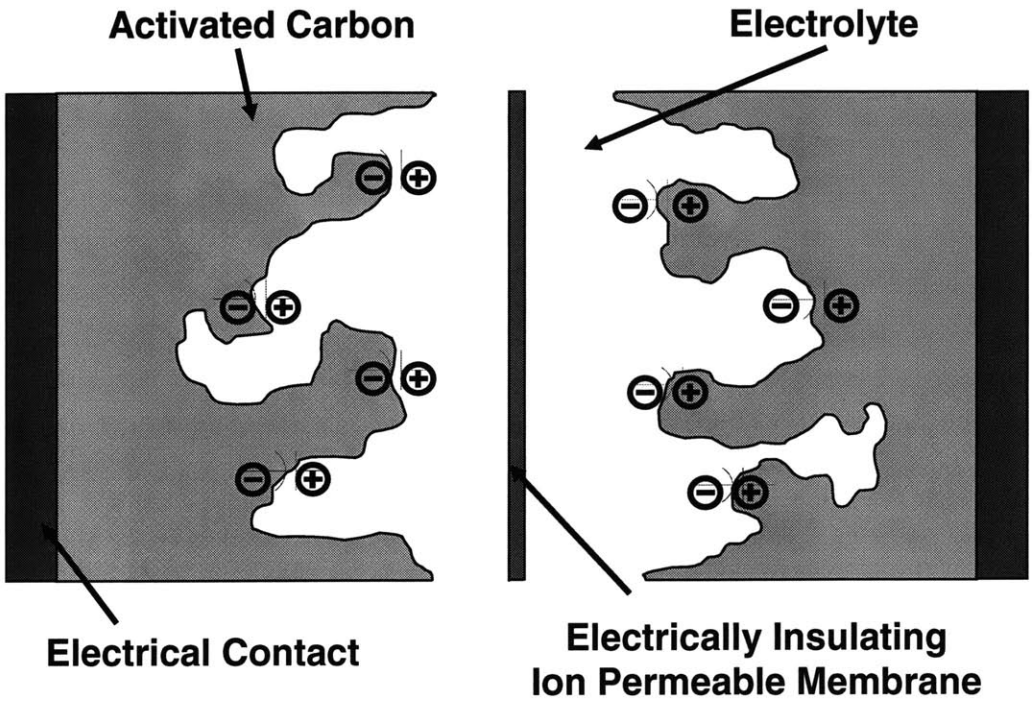

Figure 2.10: Inside a DLC (Not drawn to scale)

electrolyte ions when traveling through the electrolyte and charging the pores that must be modeled as a distributed resistance. These electrolyte resistances will be higher at lower frequencies due to the ions passing through an increased volume of electrolyte material as they attempt to populate the smaller pores.

With a seemingly infinite possibility of combinations of pore size, pore geometry, and ion paths, the exact modeling of a typical DLC would require a nearly infinite order model. This is obviously not practical. Rather the goal should be a lower order model, one that will accurately predict the behavior of the device but is not so complicated that its derivation and use would be over taxing. As the behavior of the DLC is governed by the combined effect of different time constants, the order of a general DLC model that is required to predict the performance of the device is going to be determined by its application. As an example, a third-order DLC model that is used to predict the performance of the DLC used in a pulsed power applications may not be sufficient in predicting the performance of DLCs used in an energy storage application, such as a system that may be required to depend on the DLC for an extended period of time for its energy needs (e.g., automotive key-off loads).

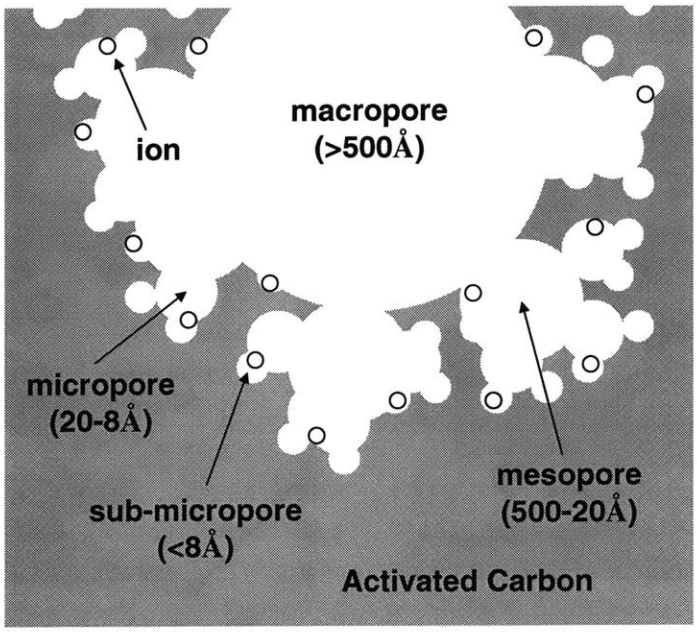

Figure 2.11: Activated Carbon Pores (Not drawn to scale) [58]

2.5 Investigating Double Layer Capacitor Models

An extensive literature survey on DLCs began in the winter of 2002. It was during this stage that investigations of the physics of DLCs, possible DLC applications, and the modeling of DLCs were initiated. Some of the most useful references for understanding the physics of DLCs and the modeling of these devices using multi-time constant networks found in this literature survey include: Conway [32], Zubieta [3, 30, 53, 54], Miller [55], Buller et al. [22], Mahon et al. [56], Kötz et al. [57], Endo et al. [58], and the material presented at the International Seminar on Double Layer Capacitors and Similar Energy Storage Devices [59, 60, 61, 62, 63, 64, 65]. It was in some of these references that the modeling efforts of Miller and Zubieta were discovered. Both researchers proposed the use of a multi-time constant network for the modeling of DLCs. We chose the simpler Zubieta model for our initial work. Of the two models, the Miller DLC model has been around longer and is more intuitive from the standpoint of understanding the physics and charge dynamics of DLCs, but may perhaps offer a higher degree of complexity than is required for the modeling of some power electronic systems containing DLCs.

It has been Zubieta's multi-time constant network and model parameter extraction procedure that has been the recent focus of this research. Zubieta has proposed that the DLC can be sufficiently modeled in some cases using only a third order system of distributed resis-

tances and capacitances, where the three time constants of the network are vastly different and the extremely long time constants, such as those on the order of days are neglected. This three time constant network has been shown to be reasonably accurate for predicting the performance of the DLC for time periods of 30 minutes or less, which for many power electronics applications will be sufficient [3, 30, 53, 54].

Zubieta's equivalent circuit for the DLC is illustrated in Fig. 2.12 [3, 30, 53, 54]. This model possesses an inductance element, a leakage resistance element, and three distributed branches (fast, τ_f; delay, τ_d; and slow, τ_s) with each branch consisting of a resistance and a capacitance term. Additionally, the fast-term branch possesses a voltage dependent capacitance term to model some of the non-linear capacitance of the device due to the interfacial tension in the double-layer [30, 31].

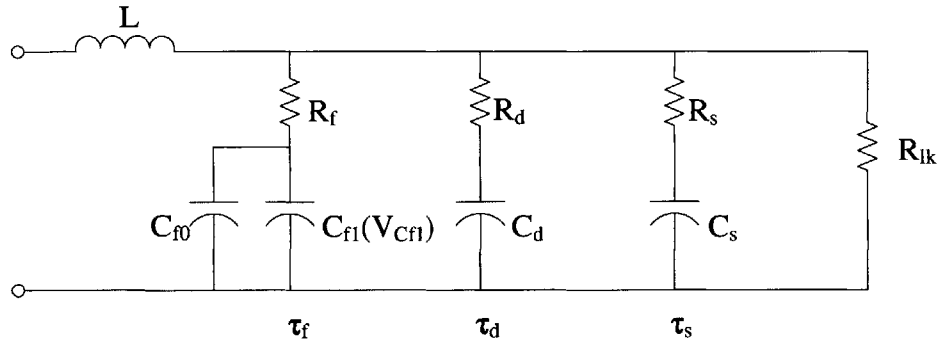

Figure 2.12: Zubieta Equivalent Circuit Model of Double Layer Capacitor [3, 30, 53, 54]

Chapter 3

Modeling of Double Layer Capacitors: Model Extraction Experiment

3.1 Introduction

The Summer 2002 MIT/Industry Consortium Project Report presented the initial results of work performed on the modeling of DLCs [66]. That report presented the idea that the behavior of the DLC was not governed by a single time constant, but in fact, that the DLC system, due to the porous electrode material used, is governed by many time constants. As an example, Fig. 3.1 compares the experimentally observed behavior of a DLC to that of a single time constant capacitor on a semi-log plot. The plot in Fig. 3.1 shows the decay in voltage (y-axis) plotted against time (x-axis). Both capacitor plots show approximately the same initial slope (as $t \rightarrow 0^+$). The single time constant capacitor plots as a linear line on the semi-log plot, whereas the DLC shows a great deal of curvature on the same plot, thus showing that the DLC needs to be modeled with multi-time constants in order to achieve an acceptable level of accuracy (relative to the time scales of interest).

The development of DLC models is a necessary step for exploiting the benefits of this technology. As with many systems, the model can range from very simple to extremely complex, depending on the required level of accuracy. The use of DLCs as a supplemental energy storage device for advanced automotive electrical systems will require the device to perform under a variety of system profiles from rapid charging/discharging (short-term storage) to long-term storage (e.g., 60 days). Figure 3.2 shows the general form of a "short-term" DLC model. The four branch model shown in Fig. 3.2 consist of a "fast" branch, a "medium" branch, a "slow" branch, and a leakage branch. The time constants of the branches (τ = RC) are assumed to be sufficiently separated and follow the relation: $\tau_f \ll \tau_m \ll \tau_s$. The Summer 2002 MIT/Industry Consortium Project Report and Winter 2003 MIT/Industry Consortium Project Report [66, 67] illustrated the development of such a model and demonstrated that the DLC can be modeled with acceptable accuracy for short-term charging/discharging as would be required for some advanced automotive electrical systems (e.g., steer by wire, regenerative braking). Those reports documented the initial work on gathering experimental long-term data (the behavior of the DLC for extended time

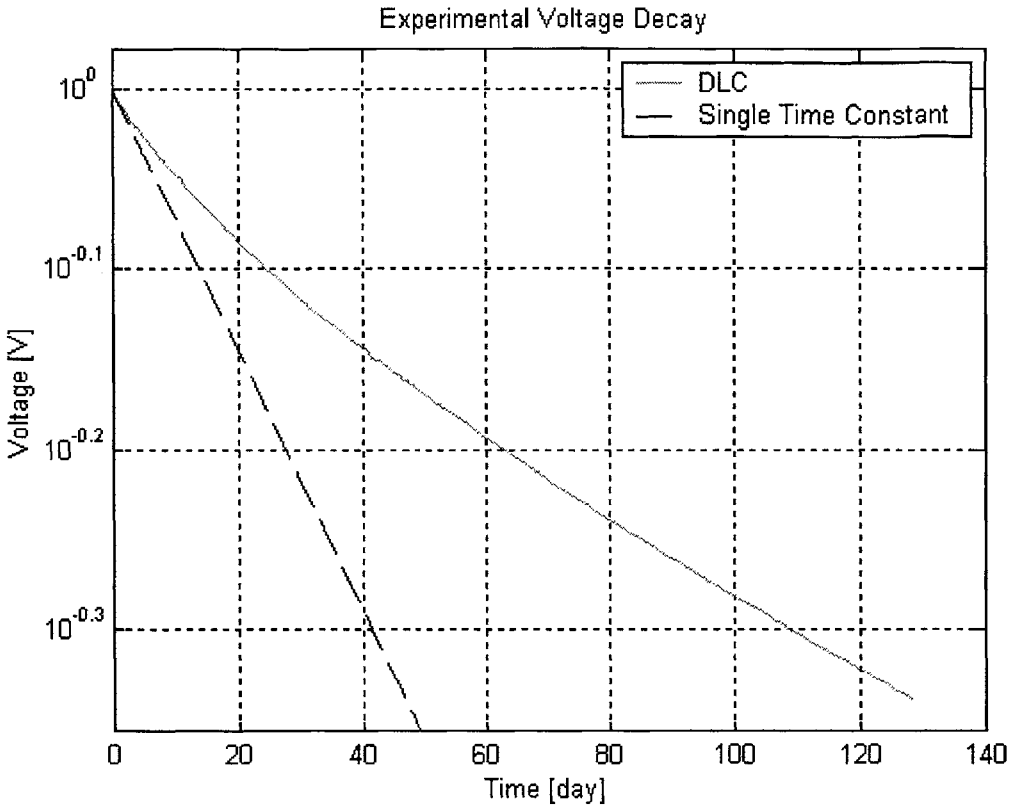

Figure 3.1: Time Constant Comparison

periods) that was used in determining an approximate value of leakage resistance for the device, and presented data that could be used to work towards the development of more complex (higher order) models that will be able to accurately predict behavior for extended time periods, as would be needed for some advanced automotive electrical systems.

The procedure used for the extraction of the model parameters for the "short-term" model is similar to the method proposed by Zubieta in his work [30], as is described in this chapter and is summarized here. Starting with a discharged DLC, the device under test (DUT) receives a pulse of constant current over a short period of time. During this time period, the "fast" branch (series combination of R_f and C_f) is charged and the terminal voltage of the device increases. It is from this period of the test that the fast branch parameters can be calculated. Figure 3.3 shows the experimental data for a DLC with a data sheet specified capacitance of 2500 F being charged from a 100 A pulse of approximately 12 s duration. The initial voltage discontinuities imply a value of R_f and the slope of the line reveals the value of C_f.

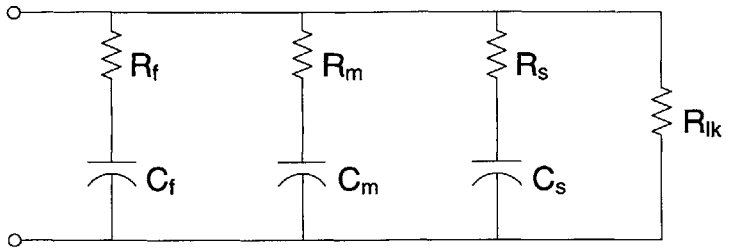

Figure 3.2: General Form of a "short-term" DLC Model

Once the pulse of current has fallen to zero and the device no longer acquires external charge, the terminal voltage begins to decay as the charge begins to redistribute itself throughout the DLC, first charging the "medium" branch (series combination of R_m and C_m) and finally the "slow" branch (series combination of R_s and C_s). The medium and slow parameters are calculated from the data points measured after the removal of the current source. Figure 3.4 shows the time period from 0 to 300 s, which illustrates the initial decay of the voltage and Fig. 3.5 shows the time period from 0 to 3000 s. It is from these extended time periods (later in the experiment) that the medium and slow branch parameters are extracted.

3.2 Test Setup

NessCap, a manufacture of double layer capacitors, donated to the MIT/Industry Consortium several 2500 F DLCs for use in developing DLC models. A test setup was assembled so that device model parameters could be determined. The test setup illustrated in Fig. 3.6 consists of a HP 6011A power supply operating as a constant current source, the DUT, a TDS 754D oscilloscope for recording voltage and current data, and an A6303 Current Probe used with an AM 503 Current Amplifier used to measure the current which charges the deivce. For the "Model Extraction" experiment, the device was charged with a constant current (of approximately 100 A) to a maximum experimental voltage (approximately 0.5 V) and then open circuited for the remainder of the 3000 s experiment.

Finally, it should be noted that the maximum voltage of 0.5 V was not arbitrary but due to the limitations of the experimental test setup. It was desired to charge the device for a time period on the order of a few time constants of the fast branch (t_f) and to minimize the charging of branches other than the fast branch. The power supply had a current limit of ~120 A. A charging current of 100 A was chosen to provide as large a current as possible while still providing a safety margin for the power supply. Assuming the device had a capacitance of 2500 F and an ESR of 0.5 mΩ (these assumed parameters are similar to those for the DUT), the capacitor in question would charge to 0.5 V in roughly 12.5 s using

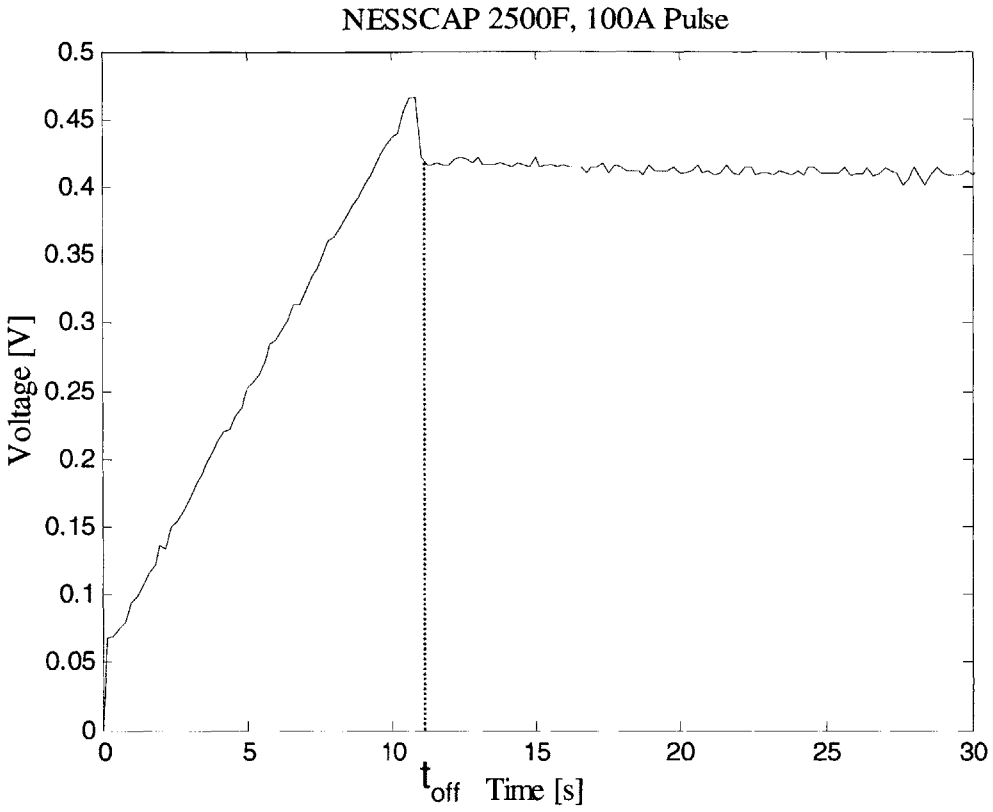

Figure 3.3: Charging and Charge Redistribution of DLC (0 to 30 s)

(3.1).

$$C = \frac{\Delta Q}{\Delta V} = \frac{I\Delta t}{\Delta V} \tag{3.1}$$

It is known that the DLC exhibits a nonlinear capacitance that is apparent when the device is charged to higher voltage levels [30]. A characterization of these nonlinearities will require a modification to the experimental setup/testing procedure.

3.3 Extraction Procedure

As mentioned above, the extraction of the various model parameters is performed at certain points along the experimental curve depending on the parameter under investigation. In order to simplify the process, we assume that initially the capacitor voltage zero and hence

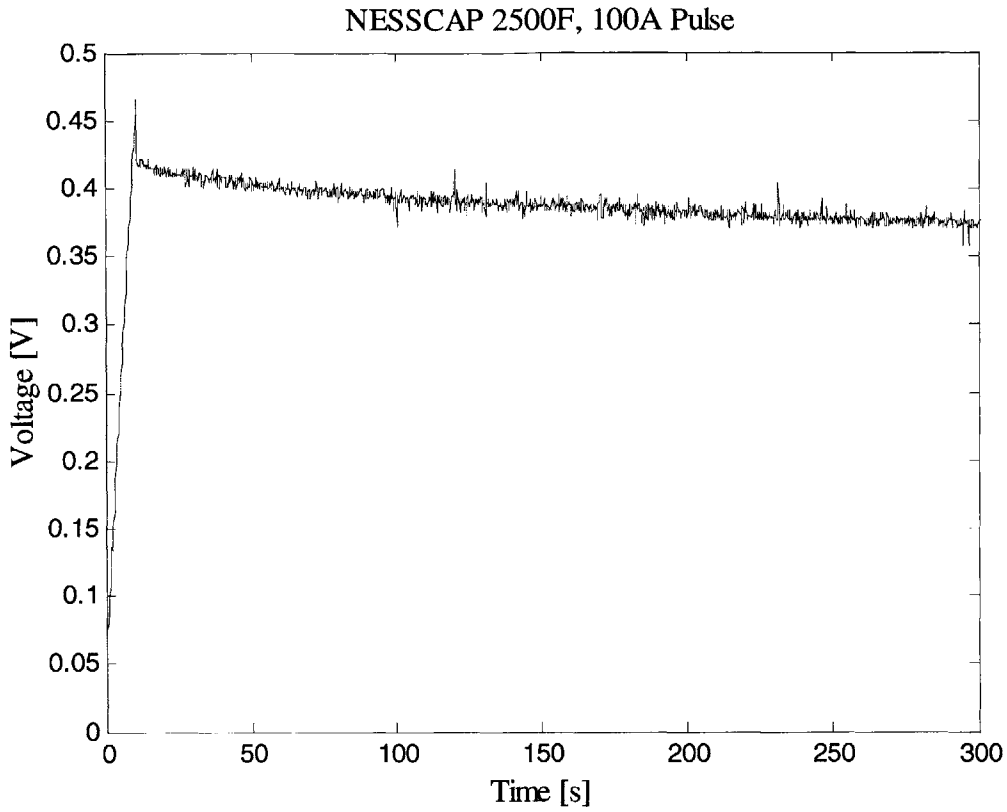

Figure 3.4: Charging and Charge Redistribution of DLC (0 to 300 s)

there is no significant charge stored in the device. Therefore, the voltages of the fast, medium, and slow capacitors are zero. Additionally, the relationship between the individual branch resistances and the individual time constants of the branches are assumed (based upon the physical properties of the electrolyte and the porous electrode structure) and presented in (3.2) and (3.3) respectively.

$$R_f \ll R_m \ll R_s \tag{3.2}$$

$$\tau_f \ll \tau_m \ll \tau_s \tag{3.3}$$

At t = 0, a pulse of constant current is applied to the device. Based on the relative resistances and time constants of the branches, the charge stored in the device during this short period of time is assumed to be stored entirely in the fast branch (one could alternatively view this process as the formation of capacitance along the surfaces of the

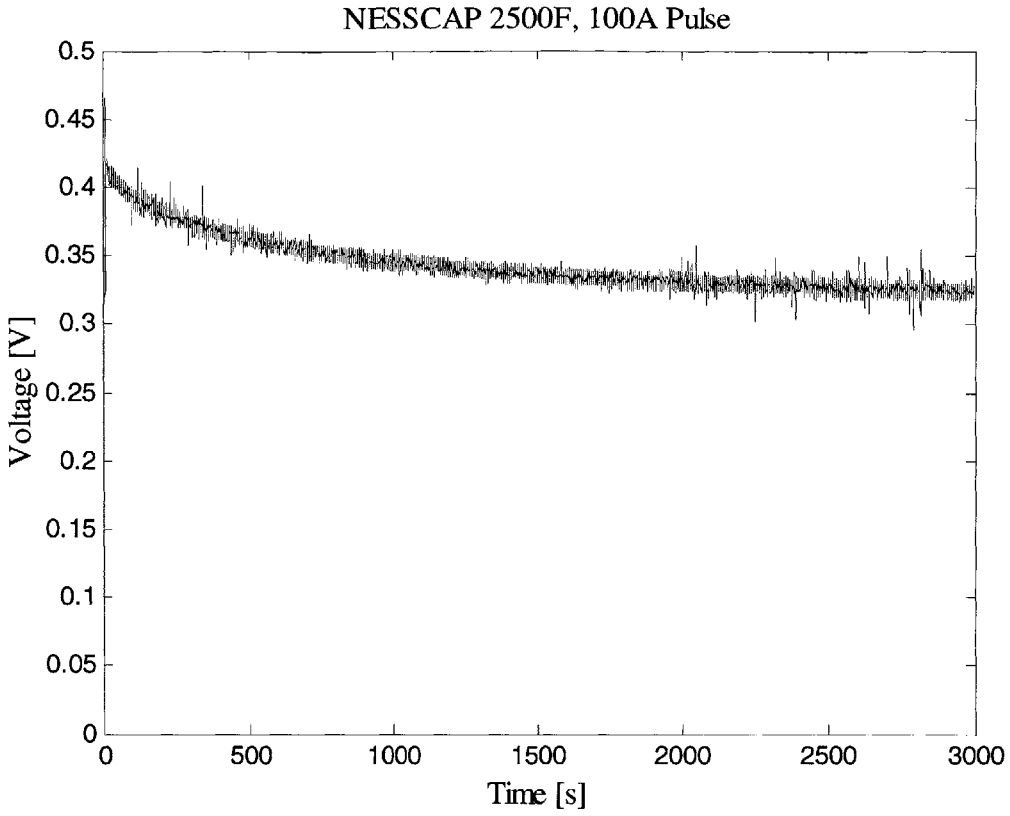

Figure 3.5: Charging and Charge Redistribution of DLC (0 to 3000 s)

larger pores of the bulk material). Figure 3.7 shows the equivalent circuit just after the current is applied to the device ($t = 0^+$). The initial step in ΔV_t shown in Fig. 3.3 is due to the resistive drop, IR_f, and thus gives the value of R_f.

Figure 3.8 shows the circuit as C_f begins to charge. It is at this point in the process that the voltage of C_f is assumed to begin to rise from its initially assumed value of 0 V. Making the assumptions mentioned above along with the assumption that the device follows a linear charge-voltage relationship, and measuring the slope of the curve shown in Fig. 3.3, the value of C_f is calculated.

With the conclusion of the current pulse, the charge begins to redistribute (diffuse) into the capacitor (this process can also be understood as the diffusion of charge into the smaller pores of the bulk). Figure 3.3 shows that just after the peak of the voltage, the voltage drops rapidly (ideally instantaneously, but finite due to the non-instantaneous fall time of the power supply) to a lower value; this change in voltage is due to the elimination of the drop across R_f. During the charging phase, the voltage measured at the terminals was the voltage of the capacitor C_f plus the voltage drop across the resistor R_f. Once the pulse has

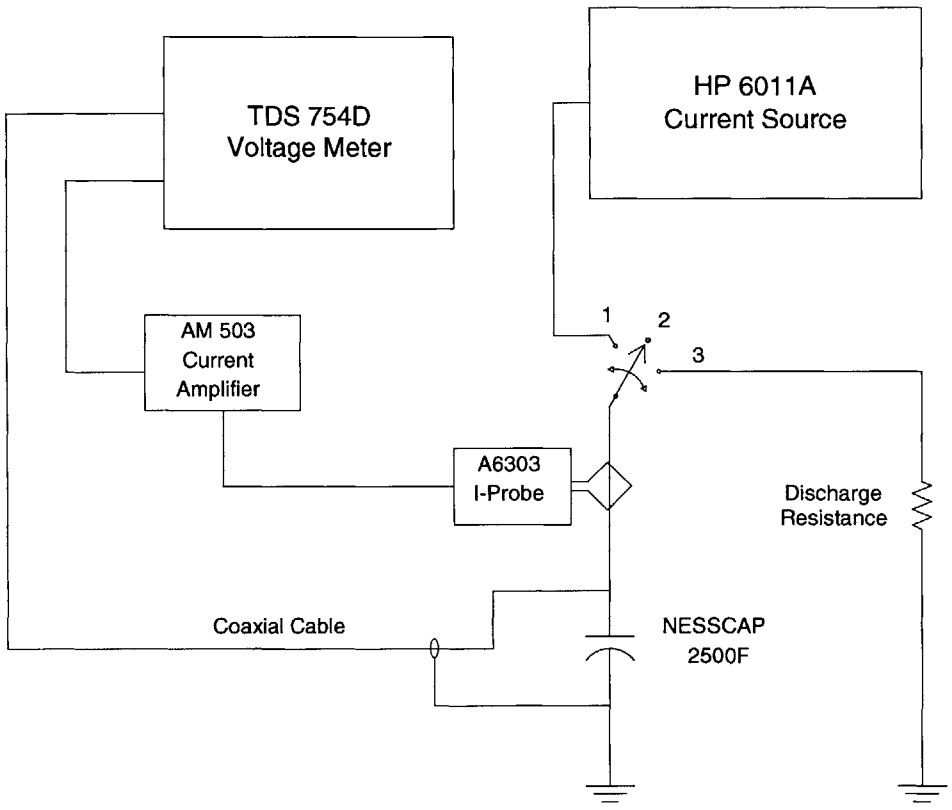

Figure 3.6: Basic Experimental Test Circuit

ended (at t = t_{off}), the measured V_t (which equals the voltage drop across the medium branch) is approximately the voltage of the capacitor C_f. Additionally, it should be noted that the voltage drop across R_f is very small (as the redistribution current, and hence the drop across R_f, are small) compared to the voltage of the capacitor C_f at this point, and the voltage of C_f can be approximated as the voltage measured at the terminals of the device. Figure 3.9 illustrates that initially the medium branch consists of only a resistor (since the initial voltage of C_m is zero) and that the voltage drop across the resistor is equal to the measured V_t and is due to the current supplied by the capacitor C_f as the charge diffuses into smaller pores. The use of (3.4) - (3.6) along with the assumptions noted above, gives the value of R_m.

$$R_f \ll R_m \tag{3.4}$$

$$R_m \cong \frac{V_t}{I_{C_f}} \tag{3.5}$$

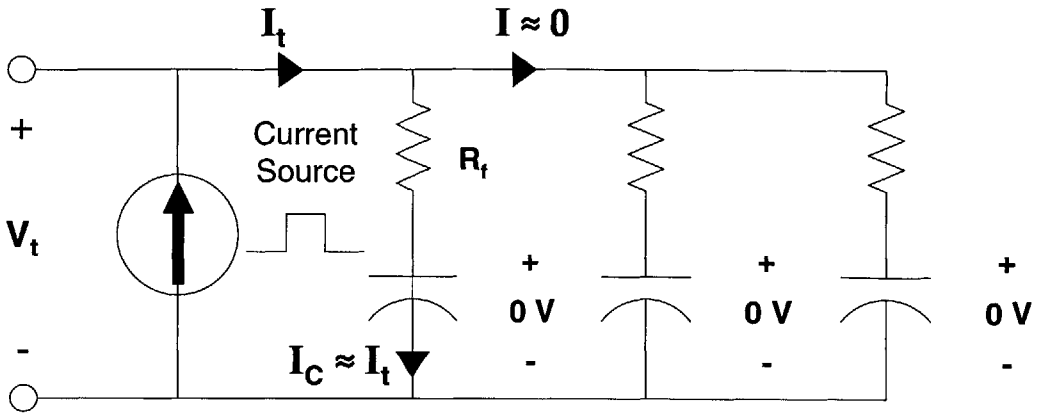

Figure 3.7: Equivalent Circuit at t=0^+

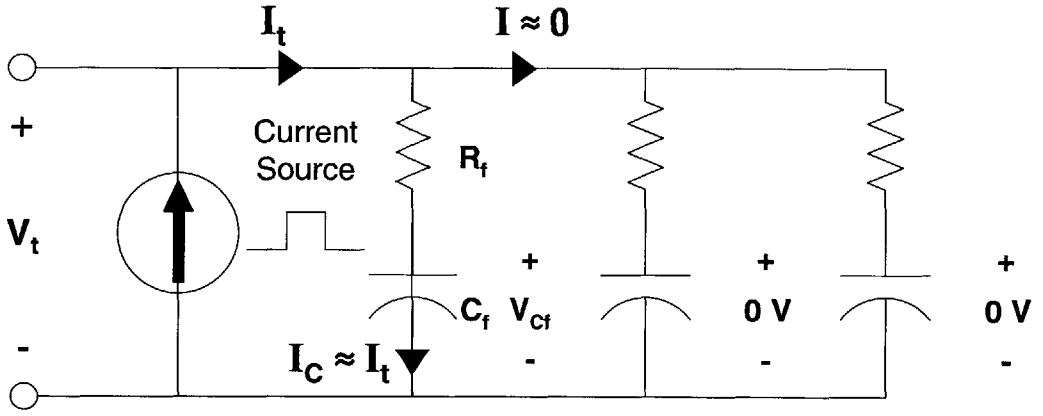

Figure 3.8: Charging of the Fast Branch ($t \ll \tau_d$)

$$R_m \cong \frac{V_t}{C_f(\frac{dV_t}{dt})} \tag{3.6}$$

Figure 3.10 represents the circuit once the pulse of current has ended and the charge has begun to flow and started to accumulate at the capacitor C_m. The voltage measured across the terminals of the device is equal to the medium branch voltage and is approximately equal to the voltage of C_f.

The current flowing in the loop illustrated in Fig. 3.10 can be viewed as a transfer of energy (charge) as the charge in C_f is reduced due to the flow of current in the loop resulting in an increase in the charge stored in C_m (as presented in (3.7) and (3.8)). Equations 3.8 - 3.10 outline the calculation for C_m making the assumption that the entire charge "lost" in C_f is stored in C_m. The value used for ΔV_t in calculating ΔQ is measured as the change

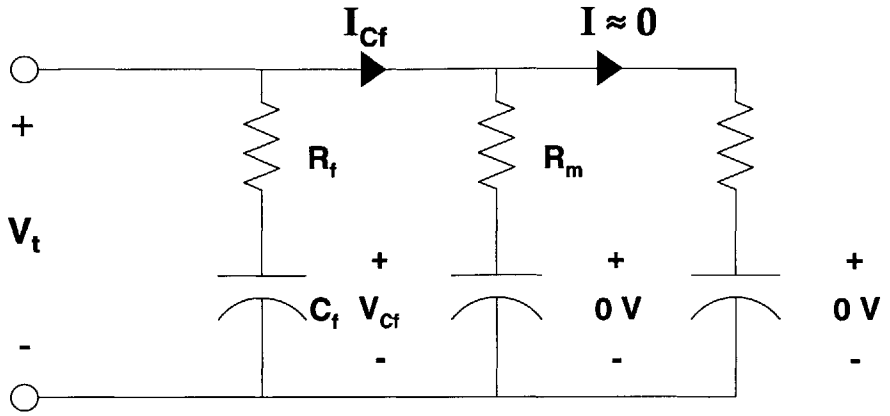

Figure 3.9: Charging of the Medium Branch, t = t^{+}_{off}

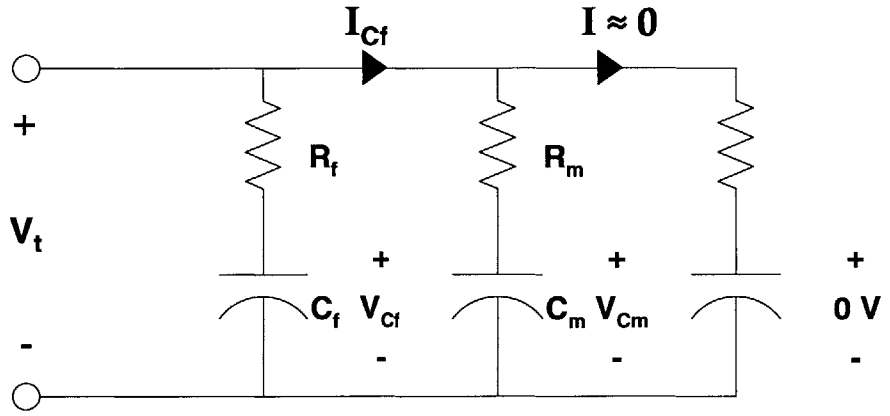

Figure 3.10: Charging of the Medium Branch, t > t^{+}_{off}

in voltage from the time just after the pulse ended until approximately 60 s later. The 60 s interval was chosen such that the interval was much greater than τ_f, much less than the assumed value of τ_s, and that the small change in voltage was measurable over the chosen interval. The value $\frac{dV_t}{dt}$ used in (3.10) is taken as the second half of the 60 s interval used in calculating ΔQ.

$$\Delta Q = \Delta V_{C_f} \mathrm{C_f} \approx \Delta V_t \mathrm{C_f} \tag{3.7}$$

$$\mathrm{C_m} = \frac{\Delta Q}{\Delta V_{\mathrm{C_m}}} \tag{3.8}$$

$$C_m = \frac{\Delta Q}{V_{C_f} - I_C R_m} \tag{3.9}$$

$$C_m \cong \frac{\Delta Q}{V_{C_f} - C_f \frac{dV_t}{dt} R_m} \tag{3.10}$$

The process outlined above is repeated for the extraction of the slow parameters (R_s and C_s). The time interval used when calculating R_s is approximately equal to 3 time constants of the medium branch, so that the medium branch is sufficiently charged before the calculation of the short branch parameters. The time interval used for the calculation of C_s is 1800 s. This long interval is chosen such that the time interval is long as compared to the assumed time constant of the slow branch, short enough that the leakage resistance can be neglected, and long enough that the change in voltage is easily measurable over the second half of the interval.

At this time, the values of the fast, medium, and slow branches have been calculated and used to generate curves to fit the experimental data. The results of this comparison are presented in section 3.4. The extraction procedure outlined above does not take into account the inductance, leakage resistance (for which in simulations we will model as very high), or voltage dependent capacitance of the device illustrated in Zubieta's model. The inductance of the prismatic DLC is assumed to be very low and the impedance due to the inductance at low frequencies may be ignored for a first-order model. The leakage resistance of the device should have very little effect on the performance of the device in pulsed-power applications as the time constant involved for that resistance would be very large.

3.4 Example of Extraction Procedure

This section provides an example of the extraction procedure presented in Section 3.3. The calculation of each of the six model parameters of Fig. 3.11 are shown in subsections 3.4.1 - 3.4.6. The derived model is then shown in subsection 3.4.7 and its performance compared to experimental data in subsection 3.4.8.

The DUT is initially discharged by short-circuiting the terminals of the device with a copper shorting bar (Fig. 3.12) for several days at room temperature. Fig. 3.13 shows the terminals of the DUT. The copper foil is placed inside the terminals of the device before stainless steel lugs are inserted to eliminate the contact resistance drop for the measurement. Coaxial cable from the TDS 745D oscilloscope is connected to the copper foil to measure the terminal

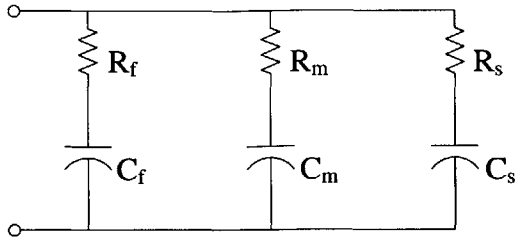

Figure 3.11: Basic DLC Model

voltage of the device. Once the device is connected to the test setup shown in Fig. 3.6 the device is charged with a constant current until the terminal voltage of the device reaches ~0.5 V. Fig. 3.14 shows the terminal voltage of the device as measured by the TDS 745D from 0 to 30 s. Figs. 3.15 & 3.16 illustrate the terminal voltage of device from 0 to 300 s and 0 to 3000 s respectively.

3.4.1 Calculation of R_f

The calculation of R_f begins with the assumption that the initial voltages of the three capacitors in Fig. 3.11 are 0 V. This assumption results in a resistive network consisting of three resistors in parallel (R_f, R_m, and R_s). Using the assumption mentioned in (1.2) the Thévenin equivalent of this parallel combination results in a resistance approximately equal to the value of R_f. Given that the network in stimulated by a source of current at t = 0 s, the resulting change in voltage at $t = 0^+$ will be directly proportional to the value of the equivalent resistance. For $t > 0^+$, the voltage of the capacitors within the network will rise from 0 V.

Figure 3.17 illustrates the pulse of current used for this experiment. The non-ideal current source exhibits a non-zero rise and fall time as well as an overshoot in current at the onset of charging. As a result of the applied current, the terminal voltage of the device responds as shown in Fig. 3.18. As mentioned in Section 3.3 and illustrated in Fig. 3.7 the resistance of the fast branch is calculated at $t = 0^+$. From Fig. 3.17 the current at this point in time is ~126 A and from Fig. 3.18 the corresponding voltage is ~0.064 V. Using (3.11) the value of R_f is found to be 0.508 mΩ.

$$R_f = \frac{\Delta V_t}{\Delta I} \tag{3.11}$$

Figure 3.12: 2500 F NessCap DLC with Shorting Bar

$$R_f = \frac{\Delta V_t}{\Delta I} = \frac{0.064\ \text{V}}{126\ \text{A}} = 0.508\ \text{m}\Omega$$

3.4.2 Calculation of C_f

In calculating the value of C_f, the assumptions that the time constant of the fast branch ($\tau_f = R_f C_f$) is much less than the time constants of the medium and slow branches, and that the resistances of the three branches follows the relation stated in (3.2) is used. Given that the charging interval is short (relative to the time constants of the medium and slow branches) the total charge delivered to the device is almost entirely stored in the fast branch capacitor.

The value of C_f can be calculated by dividing the change in charge (ΔQ_1) by the change

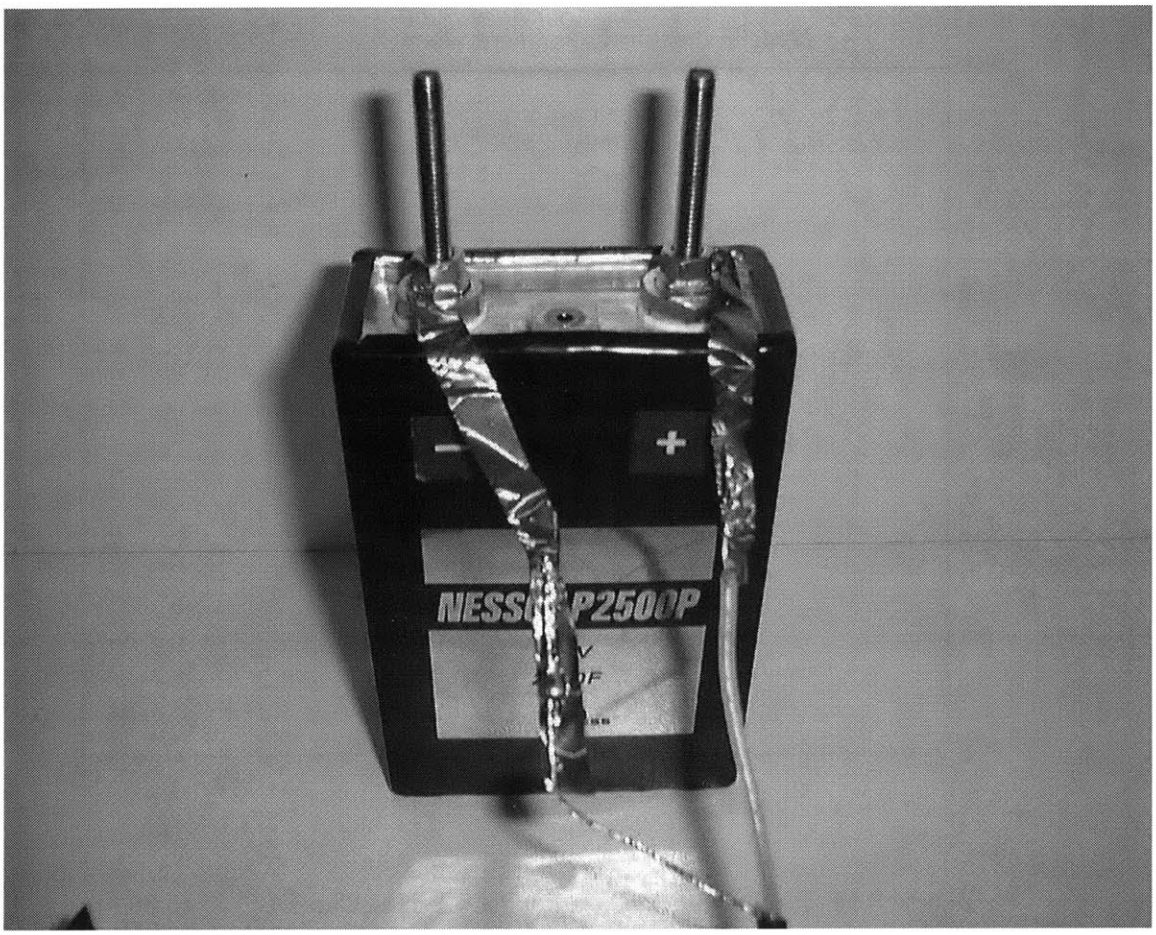

Figure 3.13: Connection of Voltage Probe to DUT

in voltage of the capacitor ($\Delta V_{C_f} \cong \Delta V_t$) over a given interval as shown in (3.12).

$$\mathrm{C_f} = \frac{\Delta Q_1}{\Delta V_\mathrm{t}} \tag{3.12}$$

The calculation of the delivered charge is found by measuring the current delivered to the DUT, the charging time, and by using (3.13) or alternatively stated, by taking the integral of the i(t) waveform shown in Fig. 3.20. The measured value of ΔQ_1 was found to be 1373.44 C and is shown as the shaded area under the curve in Fig. 3.20.

$$\Delta Q_1 = \int_0^{t=12.6s} i(t)dt \cong \Sigma(I \times \Delta t) \tag{3.13}$$

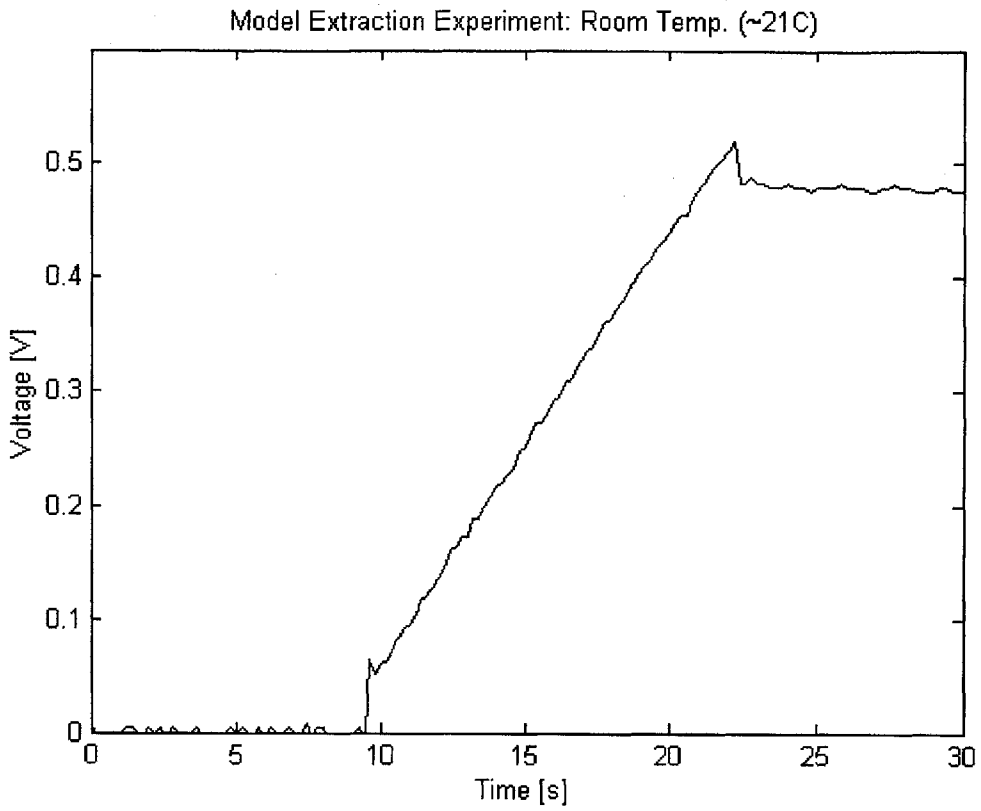

Figure 3.14: Experimental Data for 2500 F NessCap DLC (0 to 30 s)

$$\Delta Q_1 = 1373.44 \text{ C}$$

Using the change in voltage found in Fig. 3.19 during the 12.6 s charging interval (ΔV_t = 0.52 V) and (3.12), the calculated value of C_f is 2641 F.

$$C_f = \frac{\Delta Q_1}{\Delta V_t} = \frac{1373.44 \text{ C}}{0.52 \text{ V}} = 2641 \text{ F}$$

3.4.3 Calculation of R_m

The calculation of the resistance of the medium branch (R_m) is found immediately following the charging interval by using (3.14) and the assumption that the terminal voltage of the device corresponds to the voltage across R_m (i.e., $V_t = V_{R_m} + V_{C_m} = V_{R_m} + 0 \text{ V} = V_{R_m}$).

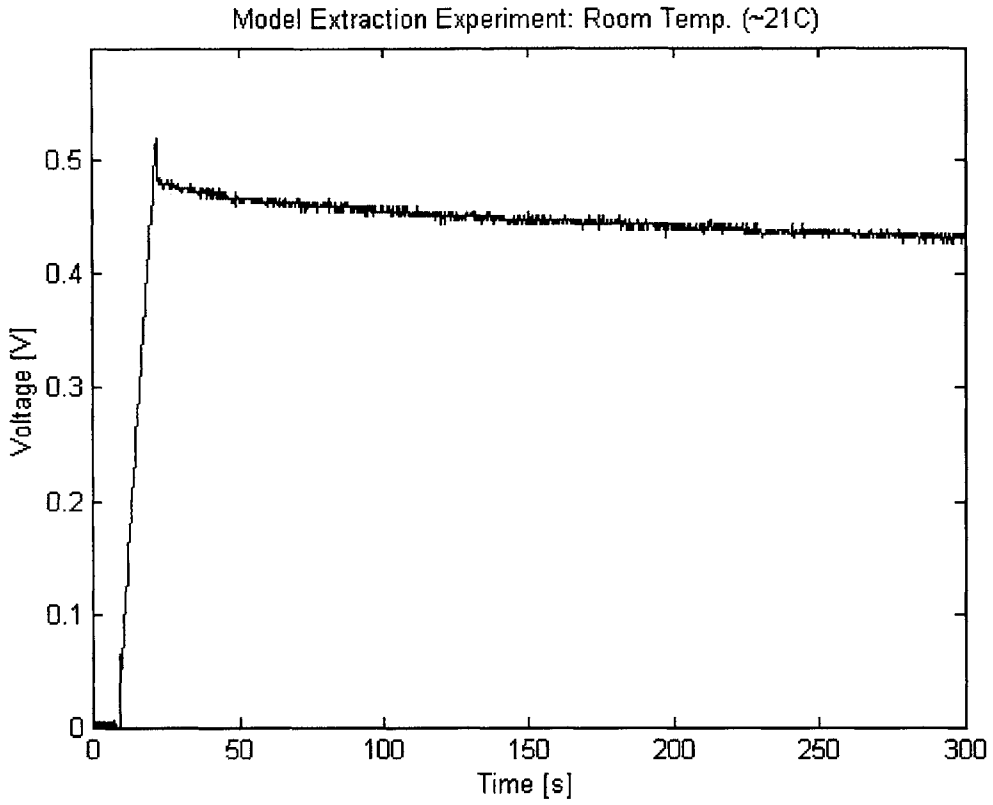

Figure 3.15: Experimental Data for 2500 F NessCap DLC (0 to 300 s)

Additionally, using the relation stated in (3.2) and basic circuit analysis (specifically, current divider theory), the relative resistance of the slow branch as compared to the resistance of the medium branch assures that the charge delivered by the fast branch is approximately equal to the charge delivered to the resistance of the medium branch (in this time interval). An additional explanation of (3.14) can be found by solving the circuit in Fig. 3.9 or by reviewing (3.4) - (3.6).

The initial decay of the voltage waveform (v_t(t)) is shown in Fig. 3.21.

$$R_m \cong \frac{V_t \mid_{t=t_{x1}}}{C_f(\frac{dV_t}{dt})} \tag{3.14}$$

The peak voltage of the waveform (V_t = 0.52 V) corresponds to the last instant that the current source was charging the device. The next data point (at t = t_4) shows that the voltage is approximately 0.484 V. The $\frac{dV_t}{dt}$ is determined by looking at the change in voltage

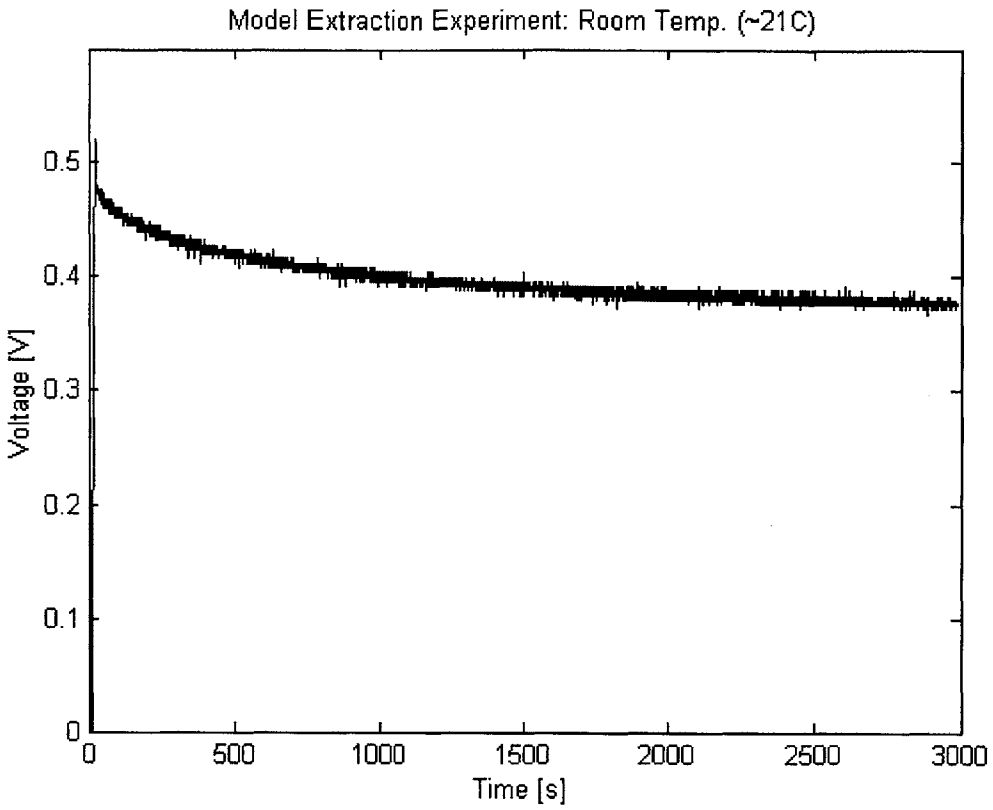

Figure 3.16: Experimental Data for 2500 F NessCap DLC (0 to 3000 s)

over a very small interval immediately following the charging period. The small dt for this calculation is important so that the voltage of C_m can be assumed to be ~0 V. Equation 3.15 shows the calculation of $\frac{dV_t}{dt}$.

$$\frac{dV_t}{dt} = \frac{V_4 - V_5}{t_5 - t_4} \tag{3.15}$$

The dt interval for this calculation was chosen to be 1 s. A straight line was extrapolated between the two points (V_4 and V_5) and the midpoint (average) voltage ($V_t|_{t=t_{x1}} = V_{x_1}$) was determined to be 0.482 V. This extrapolation was necessary due to the noise present in the experimental data and the difficulty in measuring small changes in voltage of small time intervals.

Using (3.14) and the values found above, the value of R_m was calculated as ~45.6 mΩ.

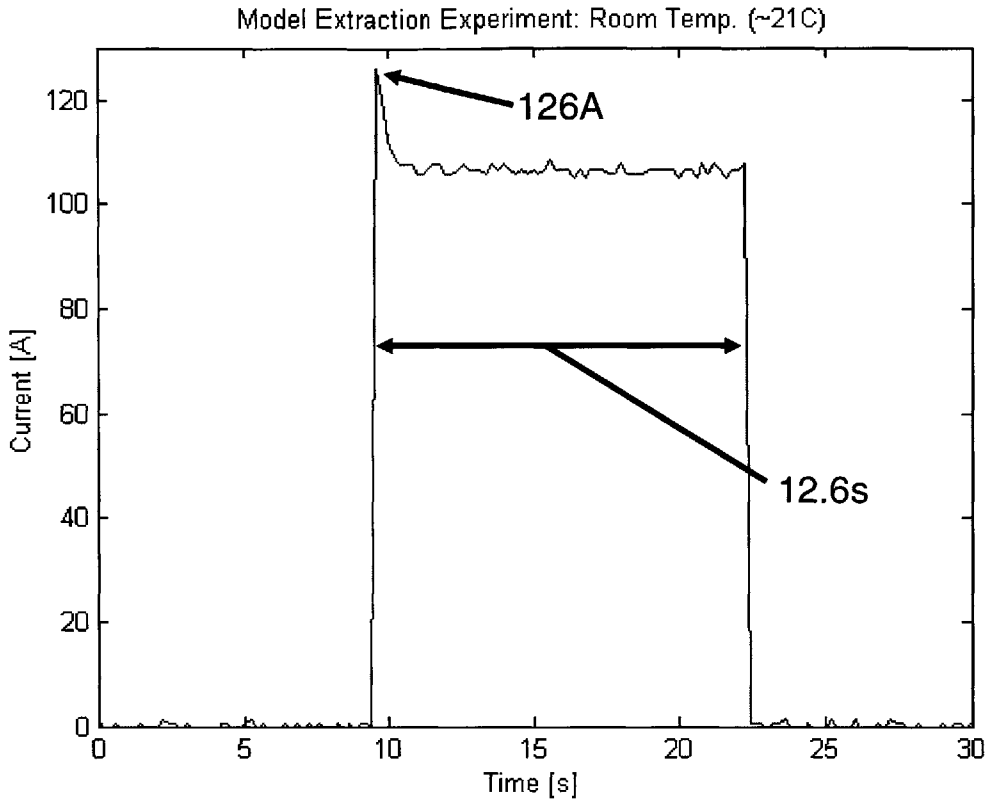

Figure 3.17: Pulse of Current used to Charge DLC

$$R_m = \frac{0.482\ \text{V}}{2641\ \text{F} \times (\frac{0.004\ \text{V}}{1\ \text{s}})} = 45.62\ \text{m}\Omega$$

3.4.4 Calculation of C_m

The value of C_m is calculated by looking at the measured voltage data following a short interval after the current source is removed. The time interval used in this case was the 60 s period following t = t_4. The 60 s interval was chosen such that the interval was much greater than τ_f, much less than the assumed value of τ_s, and that the small change in voltage was measurable over the chosen interval. The interval over which C_m is calculated needs to be sufficiently long (at least 3 times the assumed value of τ_m) to assure sufficient charging of C_m. If the interval is to long, relative to the time constant of the slow branch, the charge migrating further into the network would begin to charge the capacitor of the slow branch, thus making invalid the assumption that the charge lost by the fast branch is

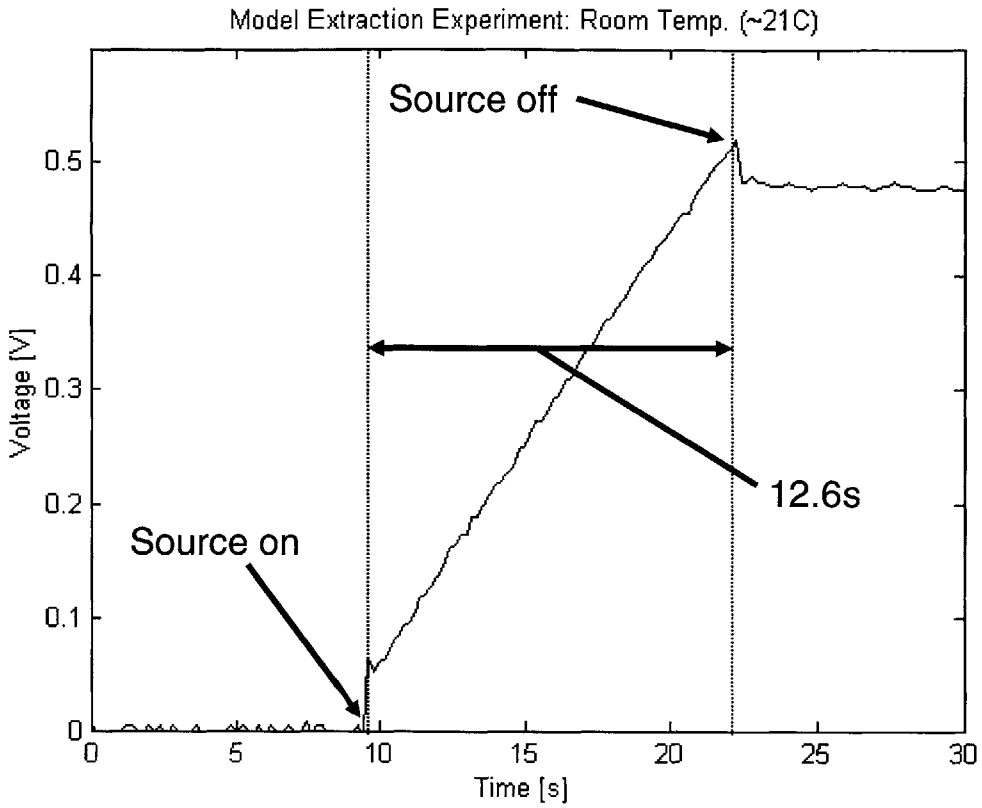

Figure 3.18: Voltage of DLC in Response to Charging Pulse

entirely stored in the medium branch.

Therefore, the change in voltage over this interval is due to the decrease in V_{C_f} ($\cong V_t$) as the charge leaves C_f to charge C_m. Equation 3.8 states that the capacitance is determined by dividing the change in charge of the medium branch (which is approximately equal to the change in charge of the fast branch) by the change in voltage of C_m. Equation 3.16 gives an expansion of this relation and uses the assumption that the sum of R_f and R_m is approximately equal to R_m.

$$C_m = \frac{\Delta Q_2}{V_{C_f|t=t_6} - C_f \frac{dV_C}{dt}|_{t=t_6} (R_m + R_f)} \cong \frac{\Delta Q_2}{V_{C_f|t=t_6} - C_f \frac{dV_t}{dt}|_{t=t_6} (R_m)} \tag{3.16}$$

The change in charge of the medium branch (ΔQ_2) is determined by (3.17) over the 60 s interval of Fig. 3.22 between t = t_4 and t = t_6. This value for ΔQ_2 is determined to be 63.384 C.

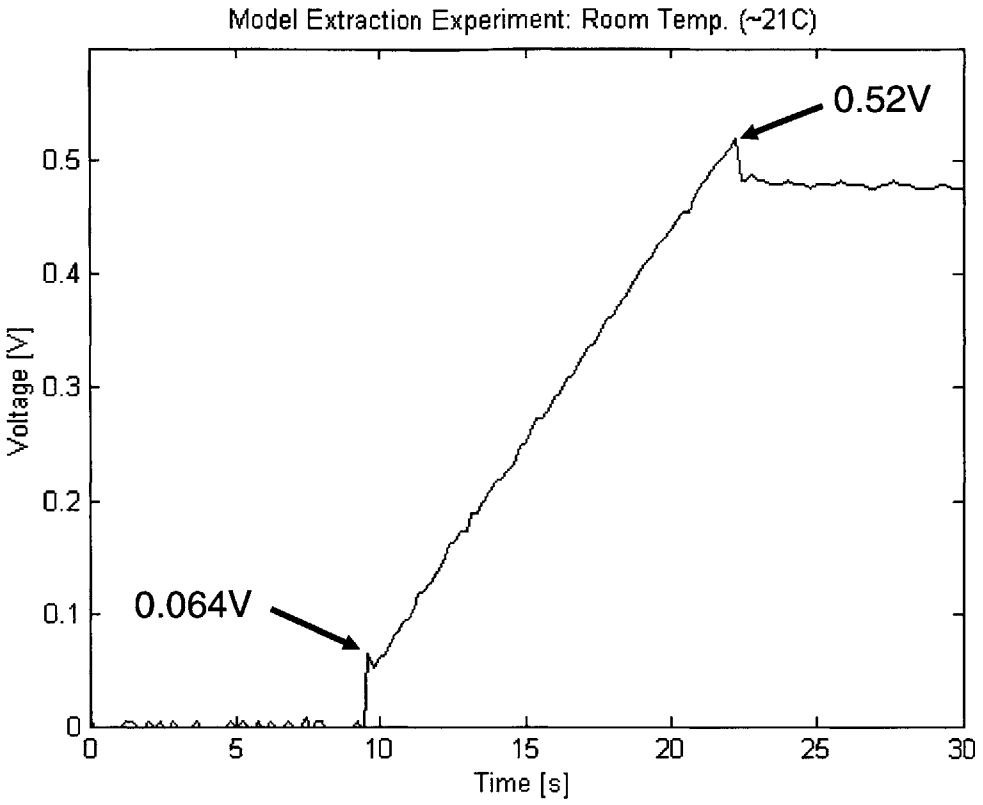

Figure 3.19: Voltage of DLC in Response to Charging Pulse

$$\Delta Q_2 = \Delta V_{C_f} \mathrm{C_f} \approx \Delta V_\mathrm{t} \mathrm{C_f} = (V_\mathrm{t}\,|_{\mathrm{t=t_4}} - V_\mathrm{t}\,|_{\mathrm{t=t_6}}) \times \mathrm{C_f} \tag{3.17}$$

$$\Delta Q_2 = (0.484\ \mathrm{V} - 0.46\ \mathrm{V}) \times 2641\ \mathrm{F} = 63.384\ \mathrm{C}$$

In calculating the $\frac{dV_t}{dt}$ in (3.18), the change in terminal voltage is assumed to be approximately equal to the change in the voltage of C_f over the dt interval. The interval used for the calculation of $\frac{dV_t}{dt}$ is the second half of the 60 s interval (of Fig. 3.22) examined when considering C_m. V_A of (3.18) is defined as the halfway point in the 60 s interval of Fig. 3.22 and the starting point of the $\frac{dV_t}{dt}$ calculation; V_6 is defined as the end of the 60 s interval and the final point used in the $\frac{dV_t}{dt}$ calculation. In examining an interval for the calculation of $\frac{dV_t}{dt}$, the interval must be such that the small ΔV can be measured by this experimental setup and a good $\frac{dV}{dt}$ measurement will be taken over a linear (in this case a nearly linear) region of the curve where the $\frac{dV_t}{dt}$ measurement ends at the point the voltage measurement for V_{C_f} is taken (i.e., at t = t_6).

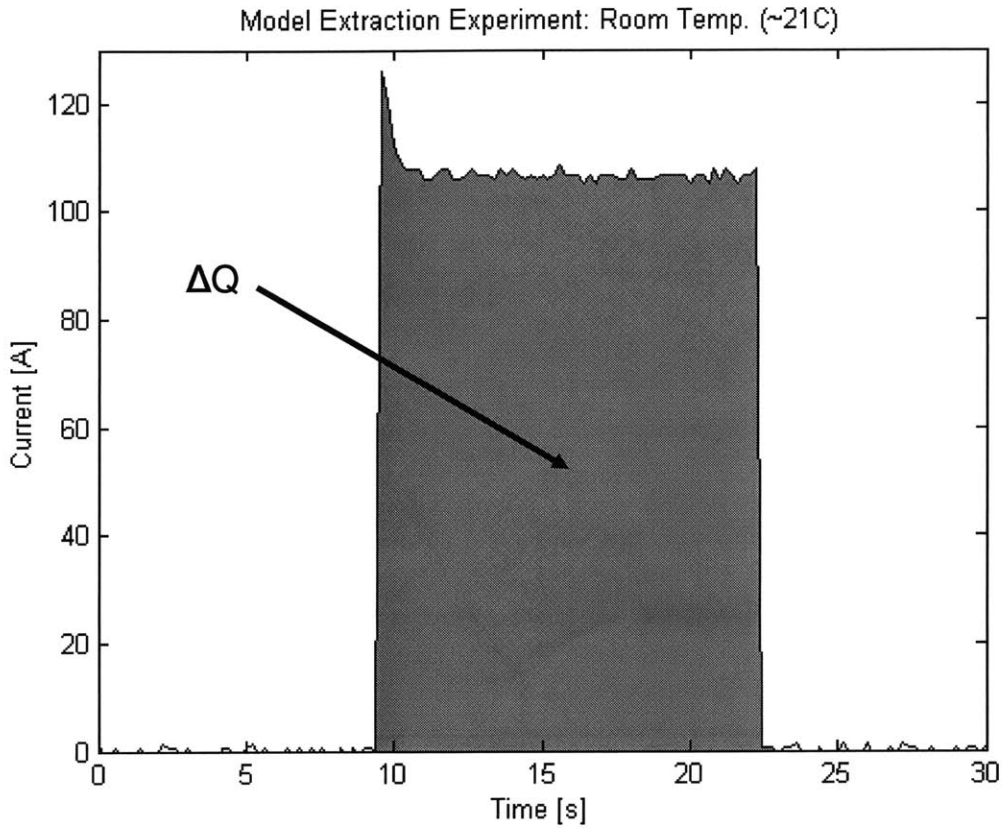

Figure 3.20: Charge (Q) Transferred to DLC

$$\frac{dV_t}{dt} = \frac{V_A - V_6}{t_6 - t_A} \tag{3.18}$$

Looking at the denominator of (3.16), the change in voltage of C_m can be found by writing KVL for the circuit in Fig. 3.10 where

$$C_f \frac{dV_C}{dt}$$

is the current in the loop and

$$C_f \frac{dV_C}{dt}(R_f + R_m) \cong C_f \frac{dV_t}{dt}(R_f + R_m)$$

is the voltage drop due to the resistances. The voltage measurement for V_{C_f} is taken at the end of the "medium charging" interval (as the voltage measurement was taken at the end

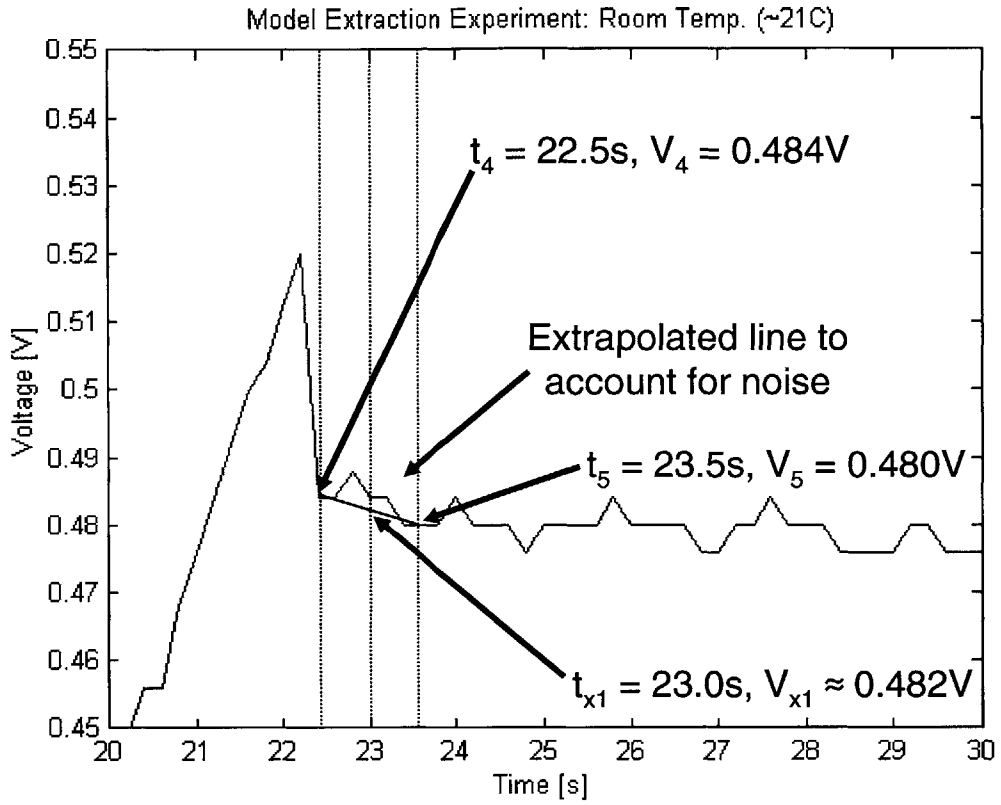

Figure 3.21: Initial Decay of DLC Voltage (20 to 30 s). Calculation of R_m.

of the "fast charging" interval for the calculation of C_f). Using these values and (3.16), the value of C_m is calculated as ~148 F.

$$C_m = \frac{63.384 \text{ C}}{0.46 \text{ V} - 2641 \text{ F} \times (\frac{0.008 \text{ V}}{30 \text{ s}}) \times (45.6 \text{ m}\Omega)} = 148.1 \text{ F}$$

3.4.5 Calculation of R_s

The calculation of the slow branch parameters is more difficult than calculating the fast and medium branch parameters due to the difficulty in measuring the small change in terminal voltage during the later times in the experiment and since the level of noise in the experimental data is more significant when measuring the small ΔV. The circuit of Fig. 3.23 is used in this subsection to solve for R_s.

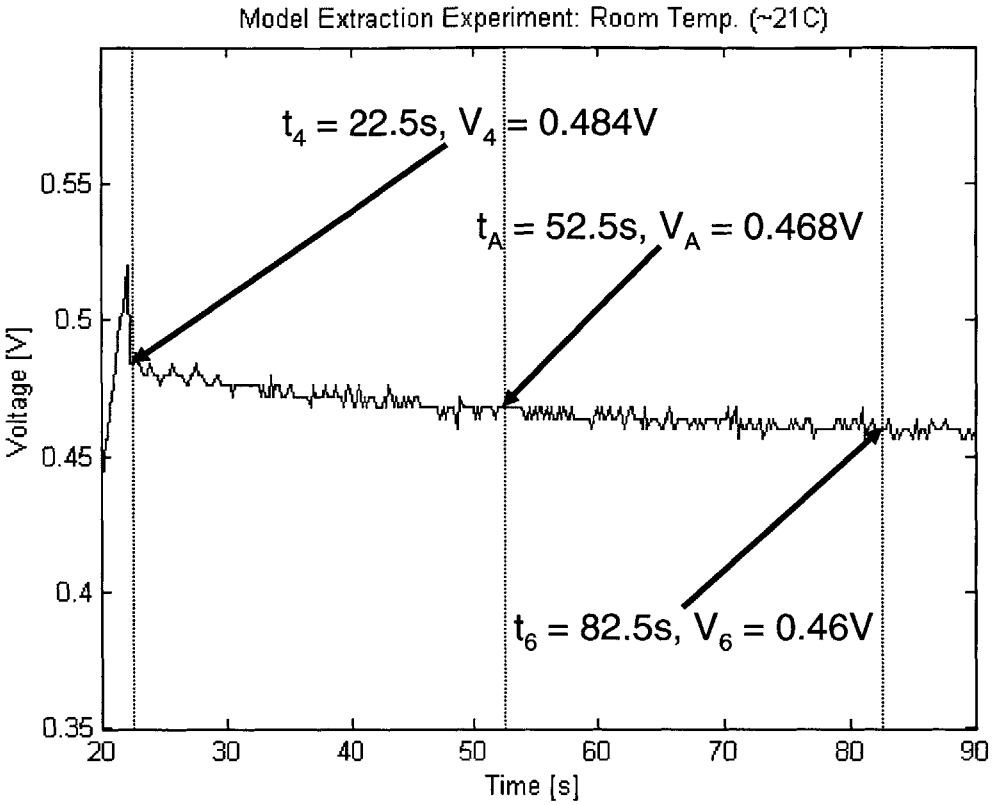

Figure 3.22: Decay of DLC Voltage (20 to 90 s). Data used to calculate C_m.

The calculation of the resistance of the slow branch begins by determining at what time in the experiment the change in terminal voltage is due to the storage of charge in the slow branch (or alternatively, to approximate at what point in the experiment the medium branch has become sufficiently charged such that the migration of charge from C_f can be said to be to charge the slow branch rather than to charge C_m.). This is done by looking at the calculated time constant of the medium branch ($\tau_m = R_m C_m \cong 6.8$ s) and looking at the voltage at $\sim 3\tau_m$ after the current source was removed from the device. The time $t = t_7$ is defined as 3 time constants of the medium branch after the current source was removed ($t = t_7 \cong t_4 + 3\tau_m = t_4 + 20$ s) and is shown in Fig. 3.24. It is assumed for this calculation that by $t = t_7$, the voltage of C_m is such that any change in voltage from this point on is due to the transfer of charge into the slow branch. Additionally, looking at the time constants of the fast and medium branches, and the relative size of capacitance of the fast and medium branches, it is assumed that the transfer of charge to the slow branch will be almost entirely from the fast branch and that the charge lost by the fast branch is almost entirely transferred to the slow branch (i.e., the medium branch is neglected).

It is assumed that at t = t_7 the voltage of C_s is approximately 0 V and that the slow branch acts as a branch with only a resistive element. Therefore, the resistance of the slow branch can be found by observing a linear change in branch voltage ($V_{s,branch} = V_t \cong V_{R_s}$) and dividing the voltage by the current in the slow branch. This relation is shown in (3.19) and the values for its calculation can be found found in Fig. 3.24. Starting with the numerator, the terminal voltage (V_t) is assumed to equal the branch voltage ($V_{s,branch} = V_{R_s}$). The denominator of (3.19) shows the current flowing around a loop consisting of the fast branch in parallel with the slow branch (the medium branch has been neglected in this calculation as mentioned above) as shown in Fig. 3.23. Additionally, the $\frac{dV}{dt}$ shown in (3.20) is measured at the terminals of the device and is assumed to be approximately equal to the $\frac{dV}{dt}$ of C_f.

$$R_s \cong \frac{V_{C_f} + V_{R_f}}{C_f(\frac{dV_t}{dt})} = \frac{V_t\,|_{t=t_{x2}}}{C_f(\frac{dV_t}{dt})} \tag{3.19}$$

$$\frac{dV_t}{dt} = \frac{V_7 - V_8}{t_8 - t_7} \tag{3.20}$$

Figure 3.24 shows that the time period used for the calculation of $\frac{dV_t}{dt}$ is 45 s. In keeping with the assumption that the voltage of C_s remains ~0 V during the calculation of R_s, a small dt is desired. As mentioned above, the change in voltage at this point in the experiment is small (and the before mentioned noise), and therefore, the dt must be large enough that the the change in voltage can be measured in the presence of the noise. Using the 45 s interval, a line was drawn between the points at t = t_7 and t = t_9. This calculation of the "average" voltage (V_{x_2} = ~0.468 V) is the same method used before to calculated R_m in Fig. 3.21. Using (3.19), the value of R_s was approximated as 988 mΩ.

$$R_s = \frac{0.464\text{ V}}{2641\text{ F} \times (\frac{0.008\text{ V}}{45\text{ s}})} = 988\text{ m}\Omega$$

3.4.6 Calculation of C_s

The final parameter to calculate for the model is the capacitance of the slow branch (C_s). In calculating this parameter, it is assumed that the change in terminal voltage ($V_t \cong V_{C_f}$) is due to the transfer of charge from the fast branch into the slow branch. As mentioned above, the change in charge of the medium branch is neglected due to the relative size of the medium branch capacitor as compared to the fast branch capacitor ($C_m \cong 0.05C_f$).

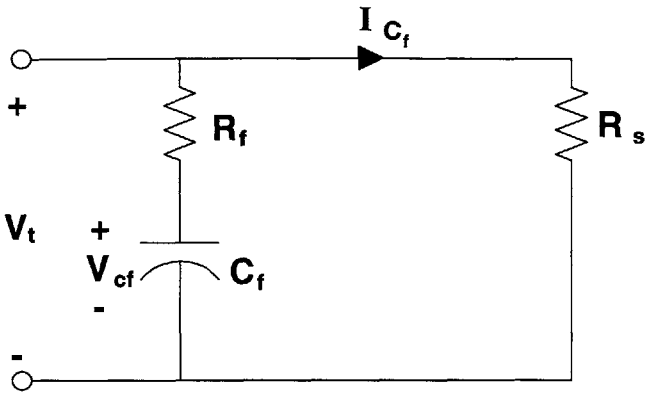

Figure 3.23: Charging of the Slow Branch

The time interval for this calculation should begin once the medium branch is charged (t = t_7) and far enough along in the experiment that the change in terminal voltage is due to the storage of charge in C_s. Figure 3.25 is used in this subsection for the calculation of C_s. Additionally, the measurement of the change in voltage at this point in the experiment is difficult, which results in the dt needing to be large. The interval chosen for this calculation is 1800 s as shown in Fig. 3.26.

The value of C_s is calculated by measuring the change in charge of the slow branch (ΔQ_3) and the change in voltage of the slow branch capacitance ($V_{s,branch} = V_{R_s} + V_{C_s} = V_t \cong V_{C_f}$) as presented in (3.21). Where R_s has been found to be much greater than R_f.

$$C_s = \frac{\Delta Q_3}{V_{C_f|_{t=t_9}} - C_f \frac{dV_C}{dt}|_{t=t_9} (R_s + R_f)} \cong \frac{\Delta Q_3}{V_{C_f|_{t=t_9}} - C_f \frac{dV_t}{dt}|_{t=t_9} (R_s)} \tag{3.21}$$

The change in charge of the slow branch (ΔQ_3) is given in (3.22); where the ΔQ of the slow capacitor is approximately equal to the ΔQ of the fast capacitor. The change in terminal voltage (ΔV_t) is approximately equal to the change in the voltage of the fast capacitor during the 1800 s interval as the value of R_f is small, the charge leaving C_f is small, and hence the voltage drop associated with R_f is negligible. Using (3.22) and the values found in Fig. 3.26, the calculated values for ΔQ_3 was found to be 211.28 C.

$$\Delta Q_3 = \Delta V_{C_f} C_f \approx \Delta V_t C_f = (V_t|_{t=t_7} - V_t|_{t=t_9}) \times C_f \tag{3.22}$$

$$\Delta Q_3 = (0.468 \text{ V} - 0.388 \text{ V}) \times 2641 \text{ F} = 211.28 \text{ C}$$

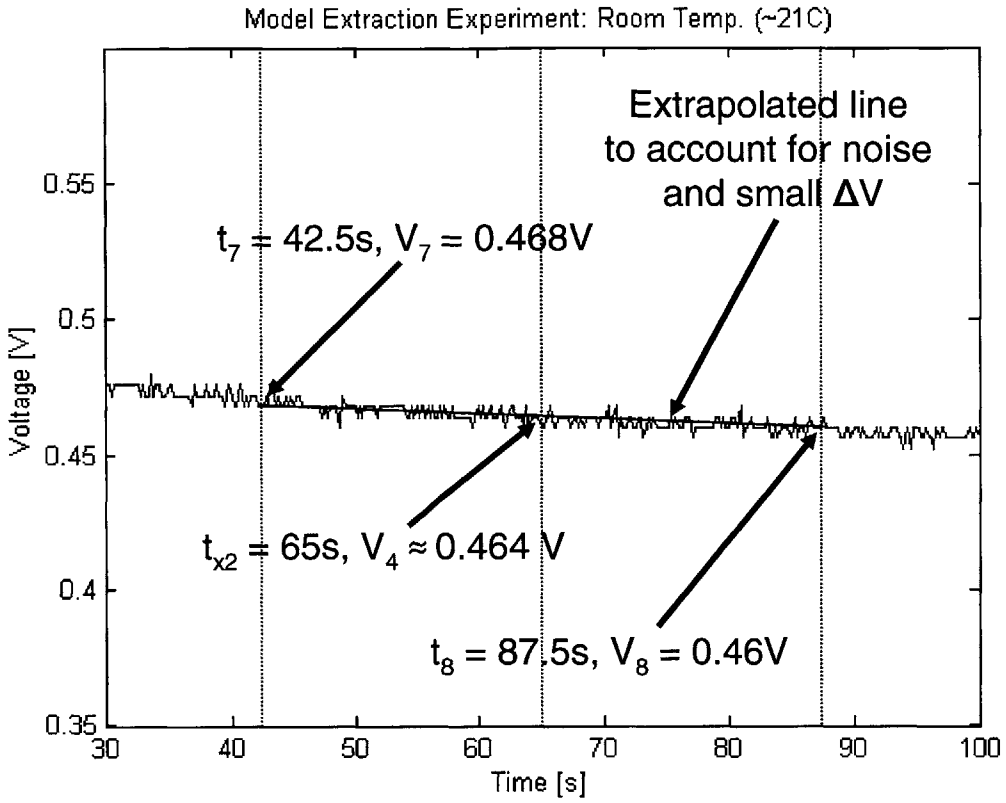

Figure 3.24: Decay of DLC Voltage (30 to 100 s). Calculation of R_s.

In calculating the $\frac{dV_t}{dt}$ in (3.23), the change in terminal voltage is assumed to be approximately equal to the change in the voltage of C_f over the dt interval. The interval used for the calculation of $\frac{dV_t}{dt}$ is the second half of the 1800 s interval examined when considering C_s.

$$\frac{dV_t}{dt} = \frac{V_B - V_9}{t_9 - t_B} \tag{3.23}$$

Looking at the denominator of (3.21), the change in voltage of C_s can be found by writing KVL for the circuit in Fig. 3.25, which consist of the parallel combination of a fast branch and a slow branch (the medium branch is neglected), and where

$$C_f \frac{dV_C}{dt}$$

is the current in the loop and

$$C_f \frac{dV_C}{dt}(R_f+R_s) \cong C_f \frac{dV_t}{dt}(R_f+R_s)$$

is the voltage drop due to the resistances. The voltage measurement for V_{C_f} is taken at the end of the "slow charging" interval (as the voltage measurement was taken at the end of the "fast charging" interval for the calculation of C_f). Using these values and (3.21), the value of C_s is calculated as ~618.5 F.

$$C_s = \frac{211.28\ \text{C}}{0.388\ \text{V} - 2641\ \text{F} \times (\frac{0.016\ \text{V}}{900\ \text{s}}) \times (988\ \text{m}\Omega)} = 618.5\ \text{F}$$

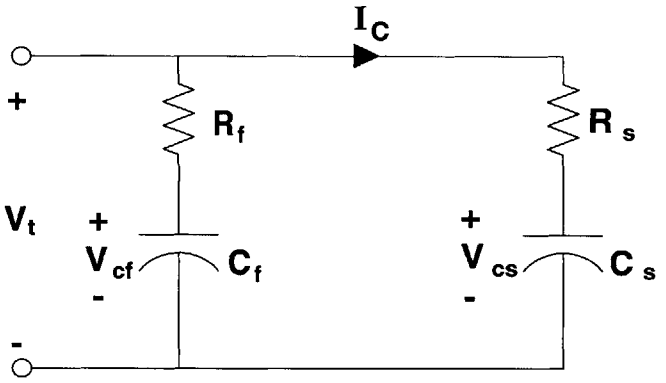

Figure 3.25: Charging of the Slow Branch

3.4.7 Extracted Model

Figure 3.27 shows the six model parameters extracted in the above example. Table 3.1 summarizes the parameters of each branches and their respective time constants. As can be seen from the results of this extraction exercise presented in Table 3.1, several assumptions made previously have been validated. Equation 3.2 stated that the resistance of the fast branch was much less than the resistance of the medium and slow branches and that the resistance of the medium branch is much less than the resistance of the slow branch. Additionally, (3.4) assumed that the resistance of the fast branch could be approximated as zero in some cases. We see from Table 3.1 that relative to the other resistances in the model, the fast branch resistance can be approximated as zero in some cases which allows the resistance of that branch to be neglected in some calculations and allows the statement that $V_t \cong V_{C_f}$ to be made in those cases. And finally, (3.3) states that the time constant of the fast branch was much less than the time constants of the medium and slow branches and that the time constant of the medium branch is much less than the time constant of the

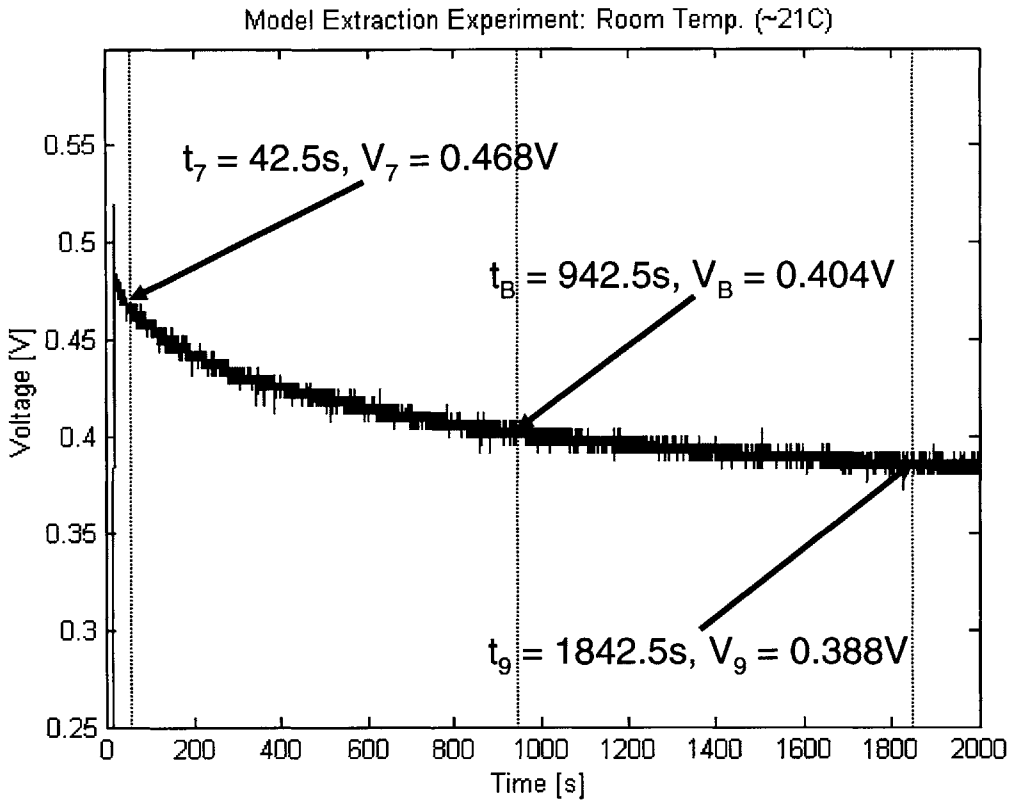

Figure 3.26: Decay of DLC Voltage (0 to 2000 s). Data used to calculate C_s.

slow branch. The question now remains as to the performance of the model with respect to the device performance.

3.4.8 Comparison of Simulated Model to Experimental Data

This subsection gives a comparison of experimental device performance with the DLC model derived above. The experimental performance of the DLC device was illustrated in Figs. 3.14 - 3.16 using Matlab®. Using the Simulink™ setup shown in Fig. 3.28 the DLC model was subjected to a pulse of current similar to that used in the lab with the actual device. The Simulink™ current pulse consists of two current sources in parallel. This configuration was used to mimic the initial overshoot of the lab current source and then a constant value for the remainder of the pulse. The fourth branch in the DLC model apparent in Fig. 3.28 is the leakage resistance branch. The value for R_{lk} used here is the value obtain for the NessCap 2500 F devices and is presented in Section 3.5.

	NessCap 2500 F DLC		
	Resistance (Ω)	*Capacitance* (Farad)	*Time Constant* (second)
Fast	0.000508	2641	1.34
Medium	0.04562	148.1	6.8
Slow	0.988	618.5	611

Table 3.1: Extracted Parameters for the 2500 F NessCap DLC Model

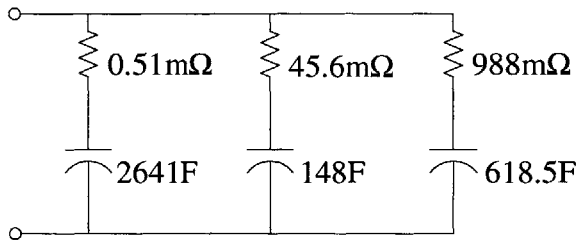

Figure 3.27: Extracted Model for 2500 F NessCap DLC

As can be seen in Fig. 3.29, the performance of the model tracks the performance of the device very well. Both curves demonstrate an initial jump in voltage due to the Thévenin resistance ($R_{Thevenin} \cong R_f$) of the device and model, and a linear rise in voltage to ~0.52 V. The values(voltage) of both curves drop once the current source is removed and continues to slowly decrease in time.

Looking on the time scale of 0 to 300 s (Fig. 3.30), the performance of the model is very good when compared to the performance of the device. Both curves are in very good agreement as the voltage decreases. Figure 3.31 shows the performance of the model and device from 0 to 3000 s. The model shows fair agreement with the performance of the device.

In conclusion, the extraction exercise covered in this section has resulted in a six parameter model of a DLC. Upon analyzing this model, many of the assumptions pertaining to the model parameters (resistance, capacitances, and time constants) have been confirmed. Additionally, Figs. 3.29 - 3.31 demonstrate that the model performs very well when simulating the performance of the device. Finally, additional adjustments of the model parameters (especially the slow parameters) can be performed to improve the fit of the model to the measured device data, but will not be shown here as the point of this exercise is to demonstrate this extraction procedure.

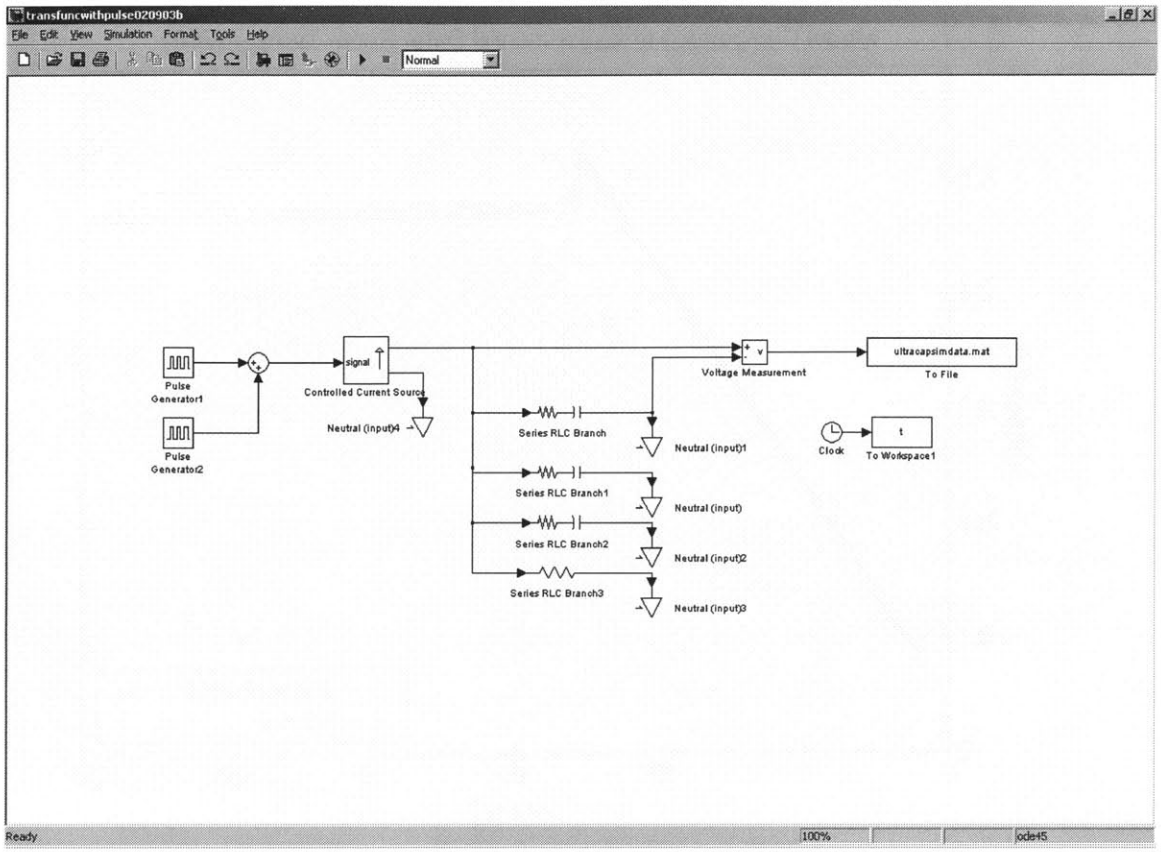

Figure 3.28: Simulink Setup

3.5 Long-Term Discharge Experiment

Figure 3.2 illustrates a seven parameter "short-term" DLC model. The extraction procedure in Section 3.3 and the example of the procedure in Section 3.4 illustrates how to derive the first six model parameters. The derivation of the seventh parameter, the leakage resistance, is discussed in this section.

As presented in the Summer 2002 MIT/Industry Consortium Project Report and Winter 2003 MIT/Industry Consortium Project Report [66, 67], a long-term discharge experiment was performed. For this study, a device was potentiostatically charged to 1 V for an extended period of time (approximately 1 week), and then open circuited and allowed to discharge (see Fig. 3.32). The idea behind this procedure was to attempt to saturate the device with charge and then observe the decrease in voltage. If the device were to be charged quickly to the maximum experimental voltage (in this case 1 V), and then open circuited, the initial voltage decay would be dominated by the charge redistribution within

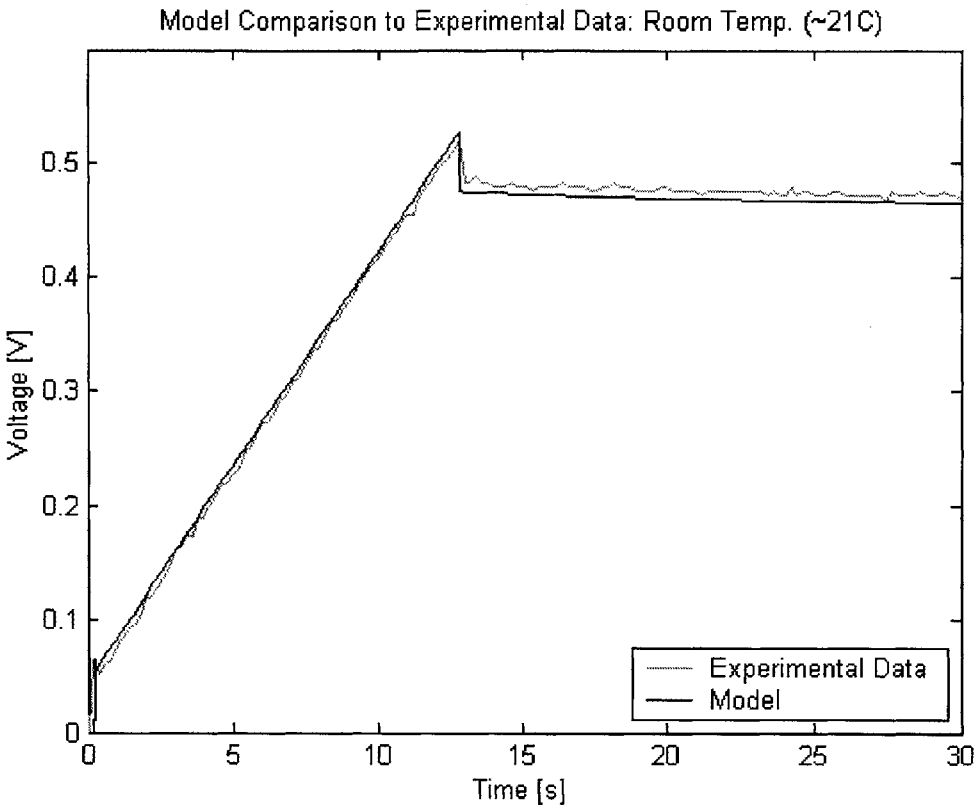

Figure 3.29: Model Comparison for 2500 F NessCap DLC (0 to 30 s)

the activated carbon electrode. On the other hand, if the device were to be charged to the maximum experimental voltage and then held there with the power supply operating in constant voltage mode (which would provide a trickle charge to account initially for the charge redistribution) until the device was saturated, the decay of voltage observed would be primarily due to the distributed leakage resistances rather than a redistribution of charge. It is the value of the "lumped" leakage resistance which we seek. It is important to keep in mind that although we are modeling the DLC as a third order system with its longest time constant on the order of tens of minutes, the device in reality is a nearly infinite order system with time constants on the order of days or perhaps even weeks. Therefore in order to minimize the voltage decay observed due to charge redistribution, the device was held at the experimental voltage for a time much greater than τ_s before being open circuited. Experimentally measured data in Fig. 3.33 shows the decay in voltage primarily due to the leakage resistances of the device.

The leakage resistance of the DLC was approximated by observing the long-term voltage decay of the device. The voltage of the device (~0.77 V) at approximately one month into

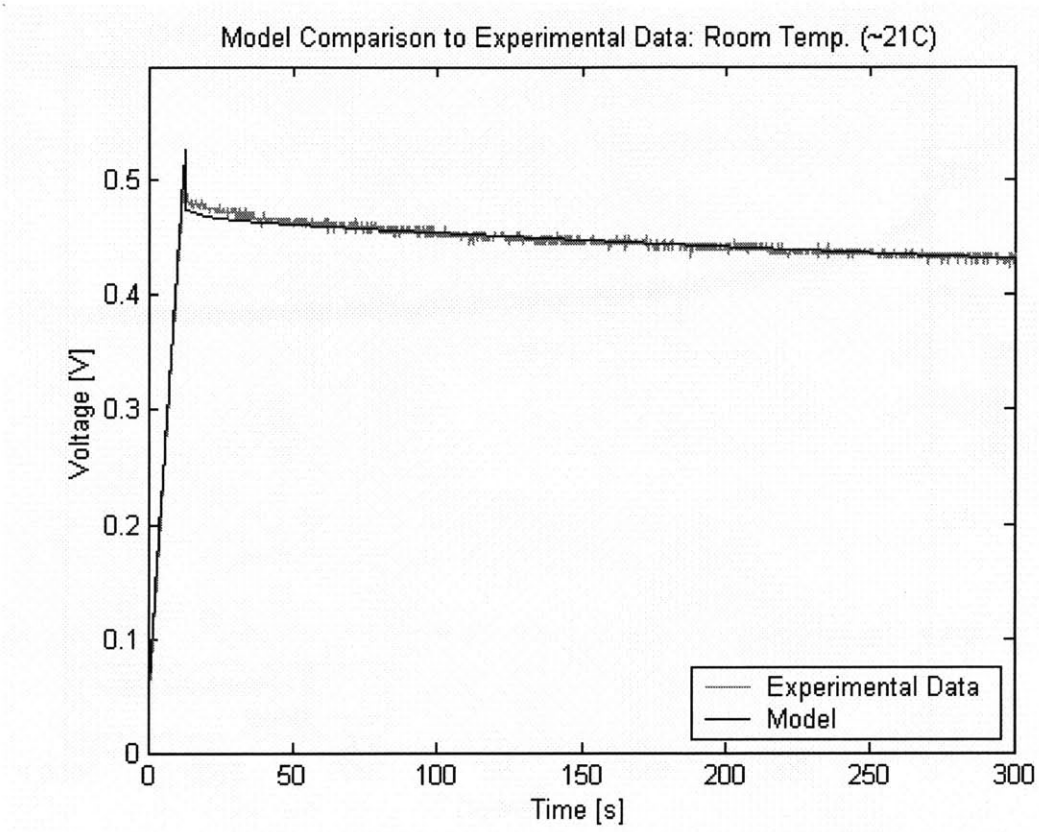

Figure 3.30: Model Comparison for 2500 F NessCap DLC (0 to 300 s)

the experiment was chosen as a matching point for the model (as seen in Fig. 3.33). The model was simulated in PSpice® for various values of R_{lk}; an approximate value of 3 kΩ was found to give comparable voltage readings at the one month matching point. It should be noted that the "short-term" model is not intended for use for time periods much more than a few hours and that for these short-term time periods, any reasonable values of R_{lk} can be found to have little impact on the results of the model. Nevertheless, an estimation of the leakage resistance was desired. The choice to match R_{lk} at the one month point results in an overestimation of the device's decayed voltage for the time period:

$$\text{more than a few hours} < T < 30 \text{ days}$$

and an underestimation of the device's decayed voltage for the time period:

$$T > 30 \text{ days}$$

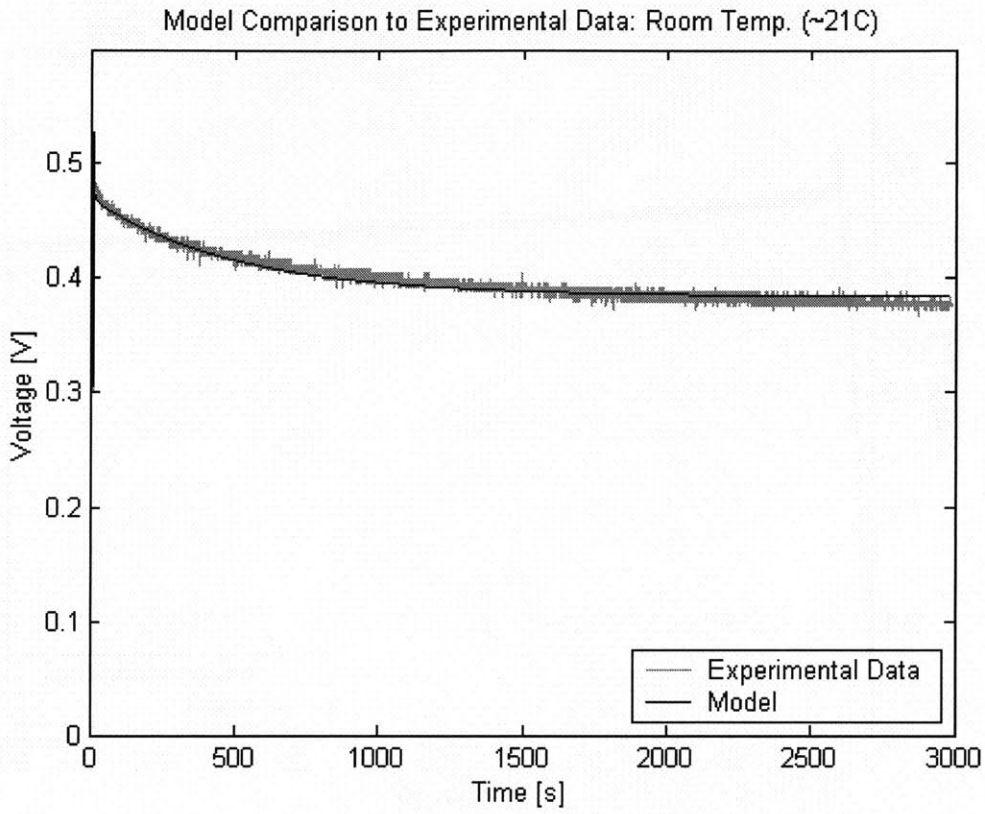

Figure 3.31: Model Comparison for 2500 F NessCap DLC (0 to 3000 s)

but reasonably predicts the device's decayed voltage at ~30 days, as would be the concern for automobiles subjected to a 30 day parking period, e.g., in an airport's long-term parking lot.

3.6 Conclusion

This chapter began with the explanation of DLC models and the need for a complex model to reasonably predict the performance of the device. The test setup used for the modeling procedure was introduced and the extraction procedure for determining the basic parameters of the model explained. An extensive example demonstrating the derivation of the model parameters from actual experimental data was presented, along with a comparison of the model's performance with the the device's performance. Finally, the derivation of a seventh parameter (the leakage resistance) was discussed along with it's significance to the model with regards to automotive applications. The seven parameter model presented in

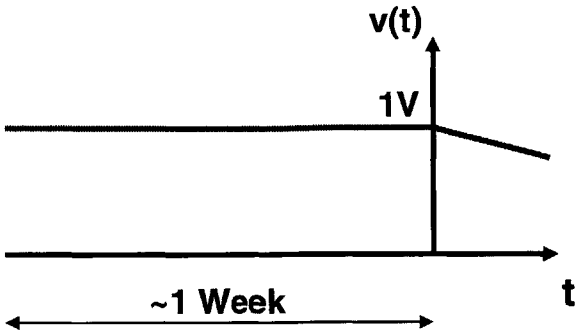

Figure 3.32: DLC Charged to and Held at 1 V

this chapter does not map the nonlinearities (voltage dependent capacitance) of the device which become apparent at higher levels of voltage, but does demonstrate the value of this extraction procedure as a base-line for DLC modeling. The seven parameter model derived above is shown in Fig. 3.34.

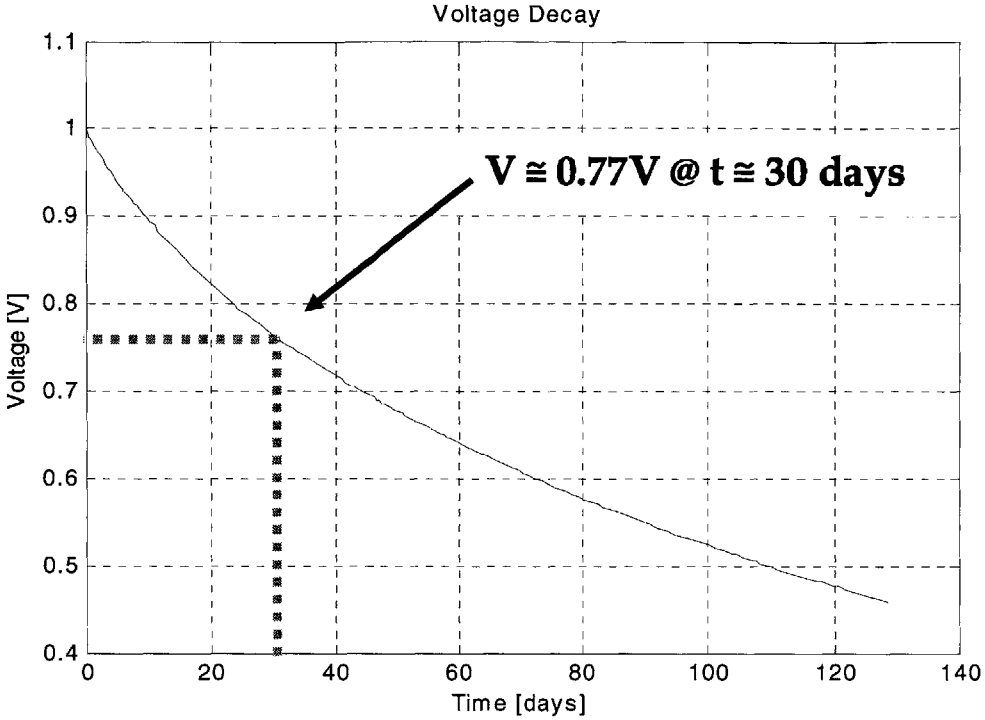

Figure 3.33: Long-Term Voltage Decay

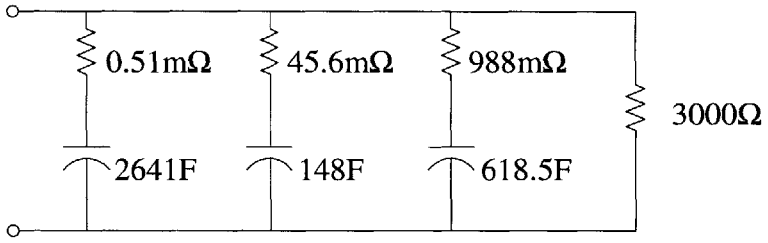

Figure 3.34: Extracted Model for 2500 F NessCap DLC with R_{lk}

Chapter 4

Validation of Modeling Procedure: Power Measurement Experiment

4.1 Introduction

To answer questions involving the energy transfer (comparing discharge energy out with charge energy in) of DLCs and to help validate the model, experimental work that measures the energy transfer of the device under test (NessCap 2500 F DLC) and computer simulations using PSpice® and MATLAB® have been performed. For the "power measurement" experiment, the device was charged to a maximum experimental voltage (approximately 0.5 V) and then discharged through a resistive load. The energy transfer was then determined by examining the experimental power data (P_{in} versus P_{out}). Additionally, to subject the device (and model) to a variety of conditions that an actual DLC might encounter, the device was 1) charged with either a high current (100 A) or a low current (10 A), and 2) discharged through the resistive load (the resistive load is defined as the resistance in the 2-gauge wire, the resistance of the connects used in the circuit, and the contact resistance of the mechanical switch used to short-circuit the device) either immediately following the point at which the device voltage reached 0.5 V, or after a delay (the delay period was determined to start once the device reached 0.5 V and end when the terminal voltage reached 0.45 V, a 10% reduction of the initial terminal voltage). The thought behind these experiments was that the actual DLC used in an automotive electrical system could be charged with a variety of currents and that the device at times would be discharged immediately following a charging session or that the device could sit for a time before being discharged. If the DLC model were to be simulated (for example in PSpice® or MATLAB®) with these different experimental profiles and could reasonably predict the actual energy transfer of the device as measured in the laboratory, then these experiments would contribute to validating the DLC model presented in this chapter (Fig. 4.3). If the device under test (DUT) had been a simpler, standard capacitor, one experiment might have been enough to validate the model. However, due to the complicated nature of the DLC (see Fig. 1.1), a constant equivalent series resistance for the device cannot be assumed and a variety of testing conditions needs to be explored to validate the model.

4.2 Test Setup

Figure 4.1 shows a diagram of the test circuit. Figure 4.2 shows the general circuit diagram of the simulation performed in PSpice® to verify the DLC model. The test circuit allows the DLC to be charged at a constant current, discharged through a resistive load, and, for experiments investigating charge diffusion, open circuited. The voltage measurements are taken across the terminals of the DLC using two voltage probes that are fed into a preamplifier and then the oscilloscope. Current measurements are taken from the line feeding current into the DLC by a current probe which is fed to the oscilloscope via a current amplifier. Experimental data can then be dumped into the computer via LabView® and filtered, plotted, and analyzed in MATLAB®. For further information on the LabView® program used, Figure B.1 in Appendix B shows a screen capture of the LabView® program that reads data from the oscilloscope for use in MATLAB®.

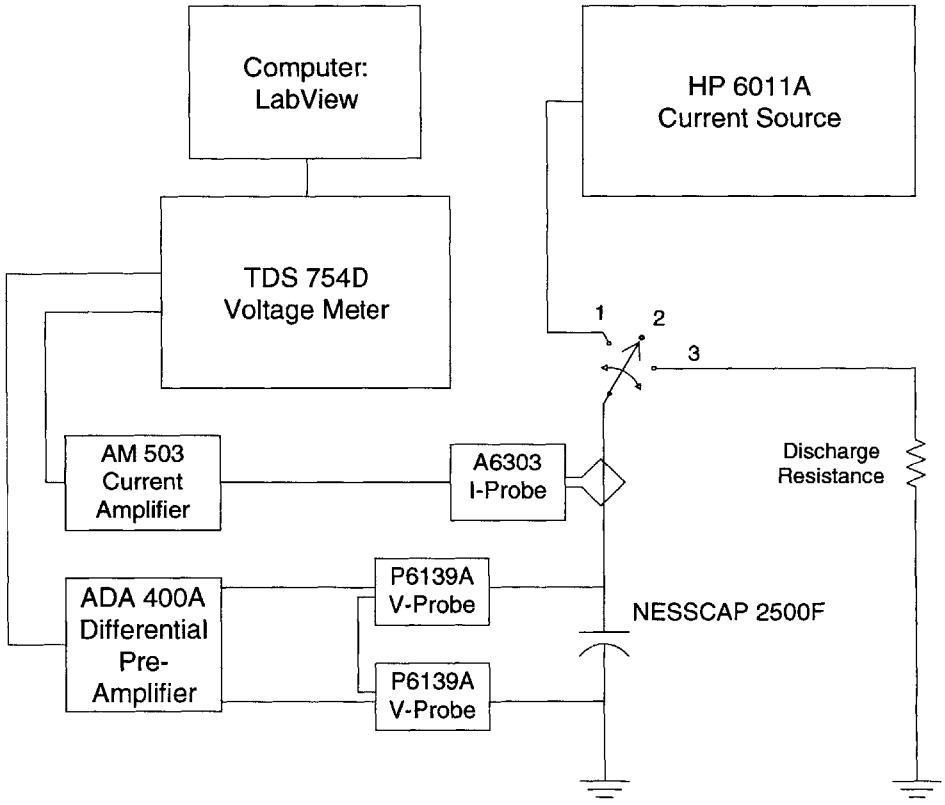

Figure 4.1: Power Experiment Test Circuit

As a final note on the test circuit used in this experiment; initially it was desired to use a circuit that would not only charge the device with a constant current, but also discharge the device with the same magnitude of constant current. The implementation of this constant

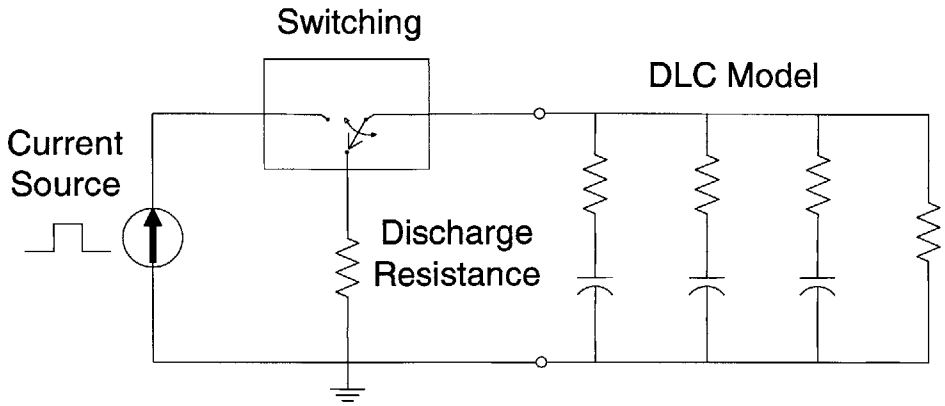

Figure 4.2: Basic PSpice® Simulation Circuit

charge/discharge circuit was investigated, but due to the time needed to modify the existing test circuit, the constant charge/exponential discharge circuit was chosen. The main difference between these two circuits is the rate of discharge of the DUT.

The measured energy transfer of the DUT is dictated by the rate of charge and the rate of discharge, hence there are a charging efficiency and a discharge efficiency that determines the total measured energy transfer of the device. The energy transfer during the charging phase of each experiment is determined by the rate of charge and the resistance of the device (simply I^2R losses); therefore a lower charging current will yield a higher charging efficiency given the same resistance. For each experiment, the maximum magnitude of the discharge current is approximately equal since for each experiment the device is discharged at similar voltages (100 A: 0.468 V; 100 A w/delay: 0.44 V; 10 A: 0.484 V; 10 A w/delay: 0.436 V; -100 A: -0.476 V), and the discharge resistance is approximately the same (a small variation in the contact resistance of the mechanical switch introduces a small variation in the total discharge resistance). Therefore given that the rate of discharge and the discharge resistance are similar, the discharge efficiency should be approximately the same in each experiment.

Table 4.1 summarizes the calculated discharge resistance of the test circuit using data from the five experiments to be discussed in this section of the chapter. Given the nature of the experimental circuit (i.e., it uses a mechanical switch), it can be seen that the contact resistance of the switch (a component of the total discharge resistance) varies a little between each cycle of the experiment (this is not applicable for the 10 A with Delay experiment as it only has one cycle). To determine the discharge resistance, the discharge current was divided into the discharge voltage as shown in (4.1). This process was repeated for each discharge cycle.

Experiment	*Summary of Calculated Discharge Resistances*				
	100 A No Delay	*100 A With Delay*	*10 A No Delay*	*10 A With Delay*	*-100 A No Delay*
Cycle 1	20.22 mΩ	24.25 mΩ	21.80 mΩ	25.26 mΩ	22.31 mΩ
Cycle 2	24.62 mΩ	23.66 mΩ	23.22 mΩ	N/A	22.53 mΩ
Cycle 3	22.04 mΩ	24.06 mΩ	23.23 mΩ	N/A	20.40 mΩ
Cycle 4	24.51 mΩ	N/A	N/A	N/A	N/A

Table 4.1: Summary of Calculated Discharge Resistances

$$R_{\text{discharge}} = \frac{V_{\text{discharge}}}{I_{\text{discharge}}} \tag{4.1}$$

4.3 DLC Model

Using the model extraction procedure outlined in Chapter 3, a model for the device under investigation was determined for use in this study's comparison. The device used in this experiment is of the same type as the device modeled in Chapter 3 (i.e., both devices are NessCap 2500 F DLCs). The model parameters extracted by the methods presented in Chapter 3 where then adjusted (resulting in the circuit seen in Fig. 4.3) for a better fit to the experimental curve and plotted again against the experimental data in Figs. 4.4 - 4.6. Figure 4.3 illustrates the general "short-term" DLC model and its extracted parameters and Table 4.2 summarizes the model parameters and time constants.

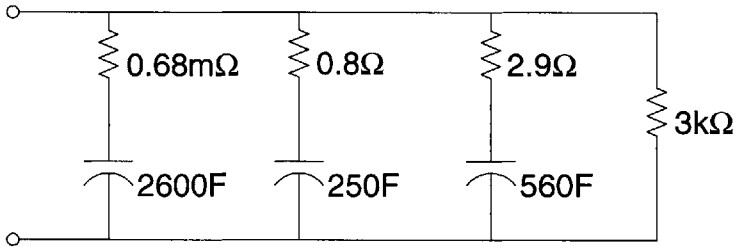

Figure 4.3: Extracted Model for 2500 F NessCap DLC

4.4 100 A Experiment

The first in a series of experiments is one that began with a discharged NessCap 2500 F DLC. The device was charged at a constant current (100 A) until the voltage at the terminals

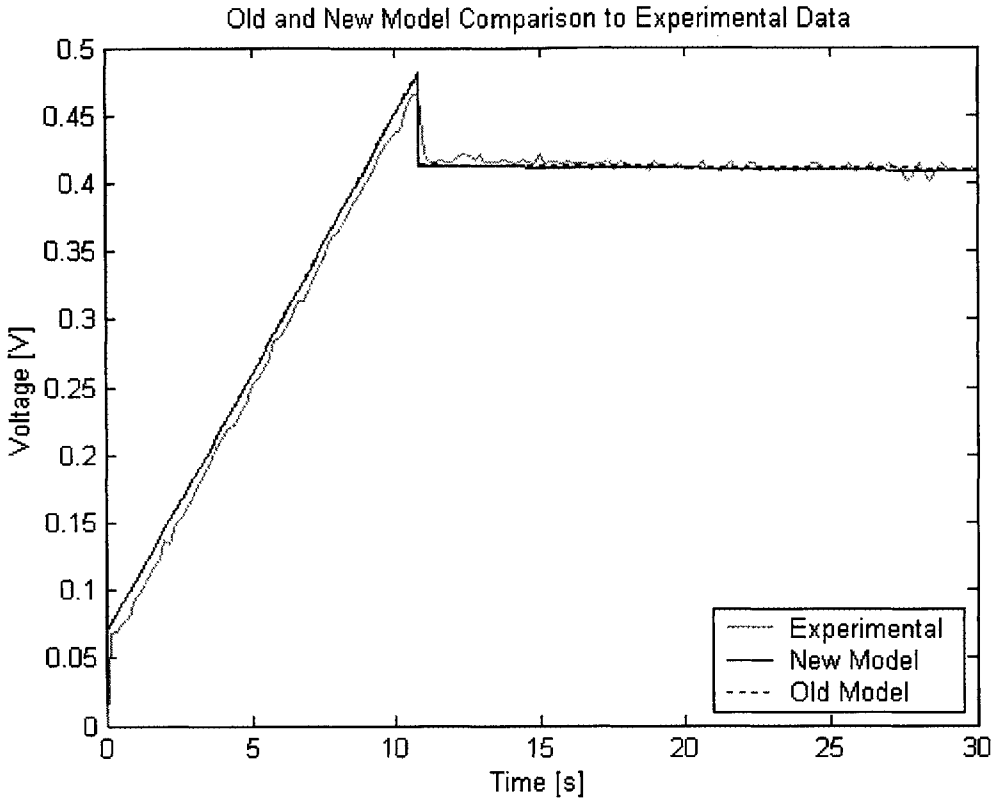

Figure 4.4: Model Comparison for 2500 F NessCap DLC (0 to 30 s)

reached approximately 0.5 V. The test circuit then transitioned from the galvanostatic charging mode to the low resistance discharging mode. Once the voltage of the device reached 0.1 V, the circuit transitioned back to the constant charging mode until the terminal voltage of the device again reached approximately 0.5 V. The transitioning voltage of 0.1 V was arbitrarily chosen for this experiment. The transition voltage could easily have been 0 V, 0.2 V or some other voltage, but a transition voltage of 0.1 V represents a significant discharge of the device before the cycle is repeated, allows multiple cycles during the experiment, and does not require the long time period that would have been required to discharge the device to 0 V.

This charging and discharging process was repeated for 4 cycles; after the 4^{th} charging phase, the device was allowed to discharge through the resistive load until the end of the experiment. The length of the experiment and the number of cycles were set such that the terminal voltage of the device would reach zero (as measured by the oscilloscope) before the end of the experiment. This particular experiment lasted 1000 s. It is important that the device voltage be allowed to reach 0 V before the end of the experiment (and hence the

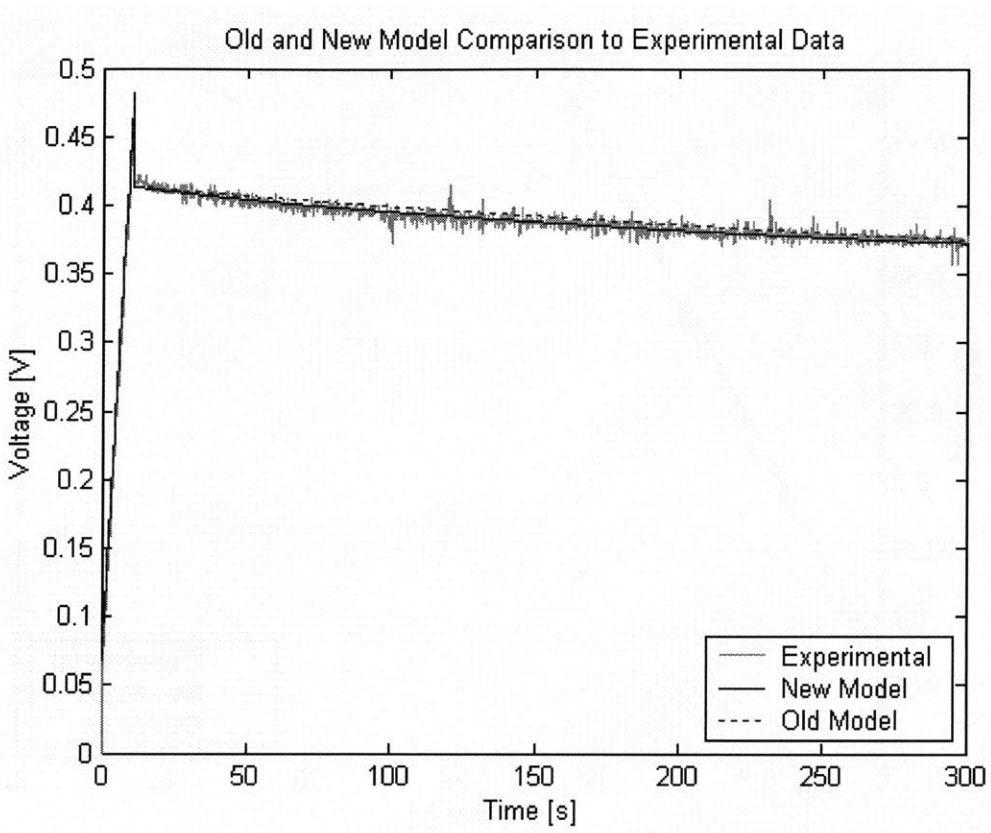

Figure 4.5: Model Comparison for 2500 F NessCap DLC (0 to 300 s)

measurements). Should the device voltage not reach 0 V before the experiment ends, the value obtained for P_{out} would be lower than what would have been obtained if the device were allowed to discharge fully, resulting in a lower energy transfer measurement than is characteristic of the device.

Figure 4.7 illustrates the data from this experiment. The voltage and current data has been filtered to remove some of the noise found in the data. The power plot was determined from the product of the filtered voltage and current data.

The experimental power data was then examined and the device energy transfer ($\frac{E_{out}}{E_{in}}$) was calculated. The data points used to generate the power versus time plot in Fig. 4.7 were imported into Microsoft® Excel to calculate the energy of the system.

$$E = \int P(t)dt = \lim_{n\to\infty} \Sigma_{i=1}^{n} P_n \Delta t \tag{4.2}$$

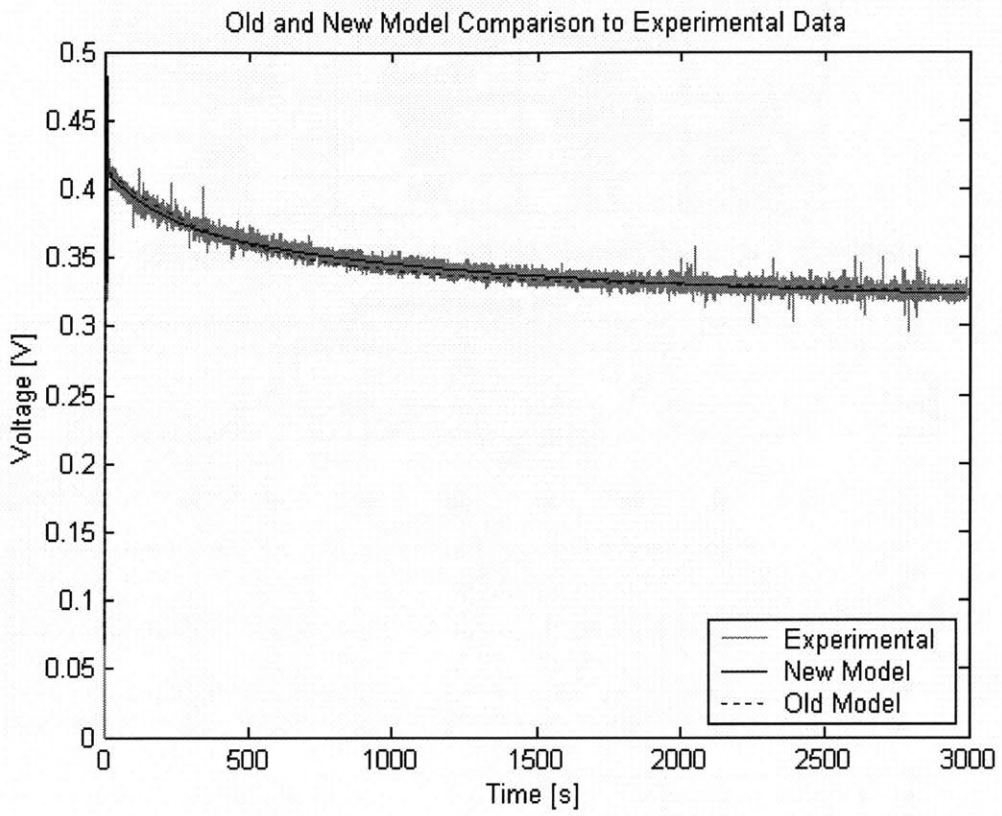

Figure 4.6: Model Comparison for 2500 F NessCap DLC (0 to 3000 s)

In (4.2), we see that the power, P, is a function of time, and the energy, E, is equal to the area under the *p(t)* curve. Additionally, we see that as the sampling interval, Δt, becomes infinitely small the sum is equal to the integral.

With a sampling rate of 5 samples per second, $\Delta t = 0.2$ s. The energy in and energy out for each of the four cycles in this experiment, as well as the total energy in and out are,

Cycle 1: $E_{in,1}$ = 371.4 J (11.2 s < t < 23.2 s); $E_{out,1}$ = -254.8 J (23.4 s < t < 124.0 s)

Cycle 2: $E_{in,2}$ = 337.1 J (124.2 s < t < 133.4 s); $E_{out,2}$ = -251.3 J (133.6 s < t < 235.4 s)

Cycle 3: $E_{in,3}$ = 335.2 J (2354.6 s < t < 244.8 s); $E_{out,3}$ = -255.8 J (245.0 s < t < 331.6 s)

Cycle 4: $E_{in,4}$ = 334.9 J (331.8 s < t < 341.0 s); $E_{out,4}$ = -267.4 J (341.2 s < t < 999.8 s)

$$E_{out} = E_{out,1} + E_{out,2} + E_{out,3} + E_{out,4} = -1029.4 \text{ J}$$

	NessCap 2500 F DLC		
	Resistance (Ω)	*Capacitance* (Farad)	*Time Constant* (second)
Fast	0.00068	2600	1.7
Medium	0.8	250	200
Slow	2.9	560	1624

Table 4.2: Extracted Parameters for the 2500 F NessCap DLC Model

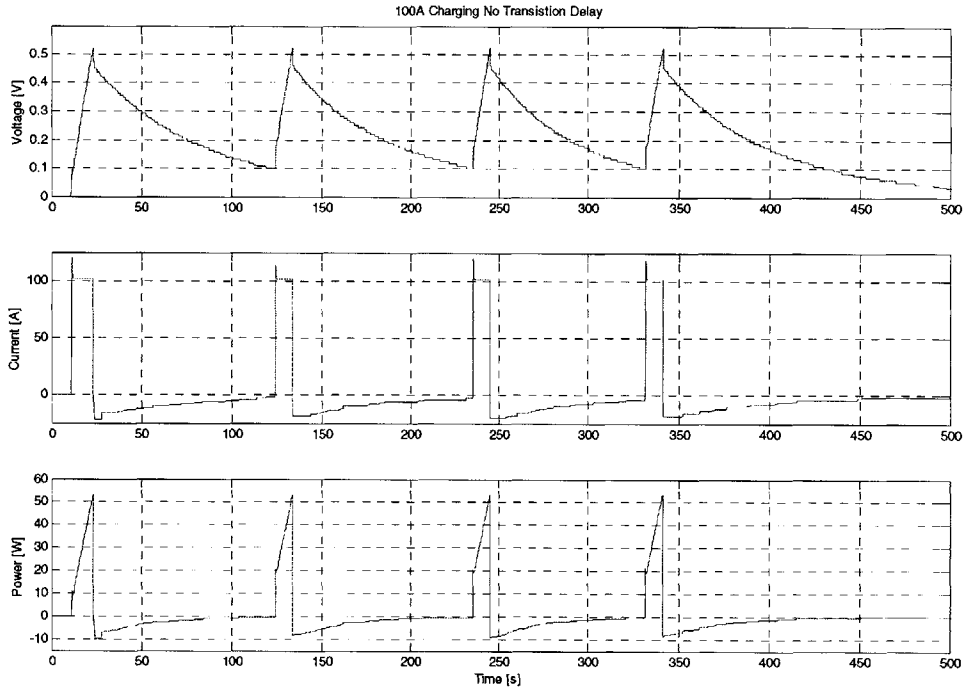

Figure 4.7: 100 A Experiment (Voltage, Current, and Power Waveforms)

$$E_{in} = E_{in,1} + E_{in,2} + E_{in,3} + E_{in,4} = 1378.6 \text{ J}$$

$$\eta = |\frac{E_{out}}{E_{in}}|*100 = 74.7\% \ .$$

The experimental energy transfer calculated was found to be 74.7%.

4.5 100 A PSpice Simulation

Once the experimental results were gathered, a simulation based on the current profile run in the lab was set up and run in PSpice® to help validate the DLC model developed

previously and to explore the idea of using PSpice® and the DLC model to predict the performance of the actual DLC device under similar experiments.

Figure B.2 in Appendix B gives the reader a detailed look at the circuit built in PSpice®. The basic circuit configuration for the simulation can be seen in Fig. 4.2. At the heart of this circuit resides the 2500 F NessCap DLC model (Fig. 4.3); multiple current sources are used in PSpice® to simulate in a piecewise fashion the current pulses supplied by the HP 6011A (a portion of the actual current overshoot of the source, as can be seen in Fig. 4.7, is also simulated here). The non-periodic switching of the circuit in the laboratory experiment has been represented by the multiple switches seen in Fig. B.2 along with multiple discharge resistances. This simulation uses four individual discharge resistances (one for each of the four cycles) to accurately simulate the change in discharge resistance for each cycle due to the variations of contact resistance of the mechanical switch.

Figure 4.8 shows the resulting voltage, current, and power waveforms of this simulation. As can be seen when comparing the current waveform of Fig. 4.8 with the current waveform of Fig. 4.7, the simulation fairly accurately reproduces the experimental waveform. Furthermore, the resulting voltage waveform (and finally the power waveform) of the DLC's response to the current excitation seems to be in fair agreement with experiment.

In an effort to calculate energy transfer for comparison with the laboratory experiments, the results of this simulation were analyzed further. Figure 4.9 details the plot of energy versus time as determined when integrating the product of the voltage and current waveform with respect to time. The maximums and minimums of the plot have been labeled as these values are needed when calculating the energy transfer ($\frac{E_{out}}{E_{in}}$).

The energy calculation for this simulation is as follows (positive changes of energy represent energy into the system, negative changes of energy represent energy out of the system):

$$\Delta E_n = E_{final} - E_{initial}$$

$$\Delta E_1 = 378.0 \text{ J} - 0 \text{ J} = 375.5 \text{ J} \ (11.2 \text{ s} < t < 23.2 \text{ s})$$

$$\Delta E_2 = 113.8 \text{ J} - 378.0 \text{ J} = -264.8 \text{ J} \ (23.4 \text{ s} < t < 124.0 \text{ s})$$

$$\Delta E_3 = 422.6 \text{ J} - 113.8 = 305.3 \text{ J} \ (124.2 \text{ s} < t < 133.4 \text{ s})$$

$$\Delta E_4 = 193.8 \text{ J} - 422.6 \text{ J} = -223.3 \text{ J} \ (133.6 \text{ s} < t < 235.4 \text{ s})$$

$$\Delta E_5 = 500.9 \text{ J} - 193.8 \text{ J} = 323.8 \text{ J} \ (235.6 \text{ s} < t < 244.8 \text{ s})$$

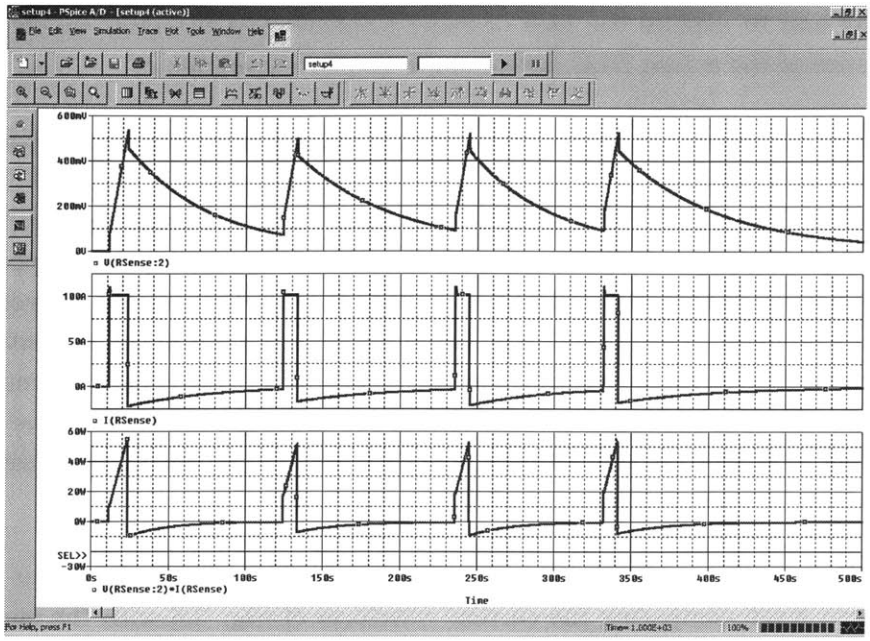

Figure 4.8: 100 A PSpice® Simulation Results (Voltage, Current, and Power Waveforms)

$$\Delta E_6 = 277.1 \text{ J} - 500.9 \text{ J} = -244.8 \text{ J} \ (245.0 \text{ s} < t < 331.6 \text{ s})$$

$$\Delta E_7 = 600.8 \text{ J} - 277.1 \text{ J} = 326.0 \text{ J} \ (331.8 \text{ s} < t < 341.0 \text{ s})$$

$$\Delta E_8 = 345.8 \text{ J} - 600.8 \text{ J} = -261.0 \text{ J} \ (341.2 \text{ s} < t < 999.8 \text{ s})$$

$$E_{out} = \Delta E_2 + \Delta E_4 + \Delta E_6 + \Delta E_8 = -993.9 \text{ J}$$

$$E_{in} = \Delta E_1 + \Delta E_3 + \Delta E_5 + \Delta E_7 = 1330.6 \text{ J}$$

$$\eta = |\frac{E_{out}}{E_{in}}| * 100 = 74.7\% \ .$$

A careful inspection of the energy delivered into the system and energy removed from the system shows an energy transfer of 74.7% for this simulation. Table 4.3 gives a detailed summary of the results of this simulation with corresponding experimental results.

An evaluation of the waveforms in Figs. 4.7, 4.8 and Table 4.3 suggests that the DLC model is able to reasonably predict (for this current profile) the terminal behavior of the actual DLC. Now, using this model we can see what is going on inside the DLC. Figure 4.10 illustrates the energy versus time waveforms for the four branches of the model presented in Fig. 4.3. The top waveform is the simulated plot for the fast branch (R_f in series with

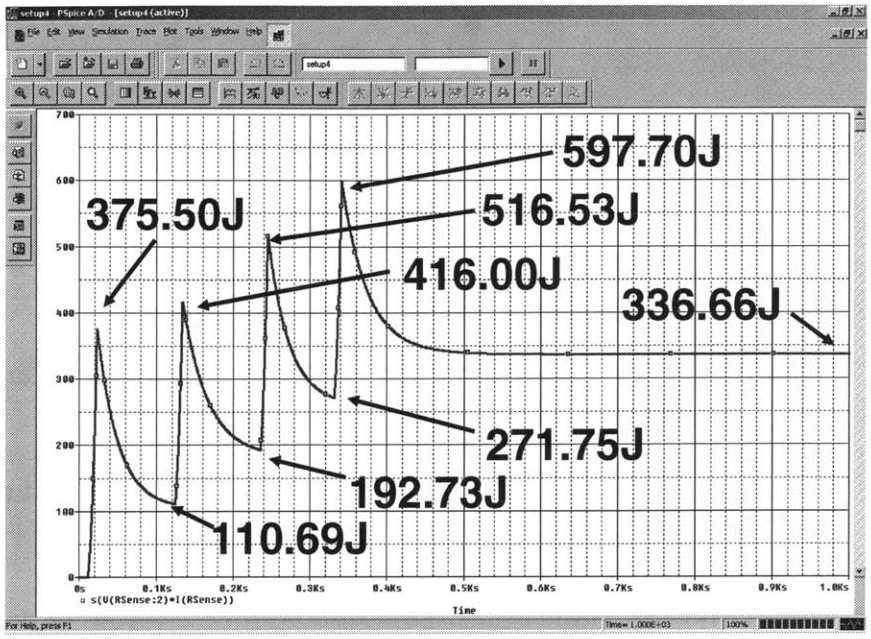

Figure 4.9: 100 A PSpice® Simulation Energy Results

C_f); the second waveform is the simulated plot for the medium branch (R_m in series with C_m); the third waveform is the simulated plot for the slow branch (R_s in series with C_s); and finally, the last waveform is the simulated plot for the leakage resistance branch (R_{lk}). Looking to the second and third plot in Fig. 4.10, we can see that a maximum energy occurs at ~380 s and ~435 s respectively and then decreases to ~16.6 J and ~8.5 J respectively. This decrease in energy in the second and third plot after reaching the maximum is a result of the stored energy in the medium and slow capacitances being removed from the respective branches during the discharge of the branches. The fourth plot in Fig. 4.10 shows that the energy reaches a maximum of ~9.2 mJ and stays constant, as would be expected for a

Summary of Experimental/Simulation Results for 100 A Test					
Measured in Lab	*Energy In*	*Energy Out*	*Simulated in PSpice®*	*Energy In*	*Energy Out*
Cycle 1	371.4 J	-254.8 J	Cycle 1	375.5 J	-264.8 J
Cycle 2	337.1 J	-251.3 J	Cycle 2	305.3 J	-223.3 J
Cycle 3	335.2 J	-255.8 J	Cycle 3	323.8 J	-244.8 J
Cycle 4	334.9 J	-267.4 J	Cycle 4	326.0 J	-261.0 J
Total	1378.6 J	-1029.4 J	Total	1330.6 J	-993.9 J
Energy Transfer	74.7%		Energy Transfer	74.7%	

Table 4.3: Summary of Experimental/Simulation Results for 100 A Test

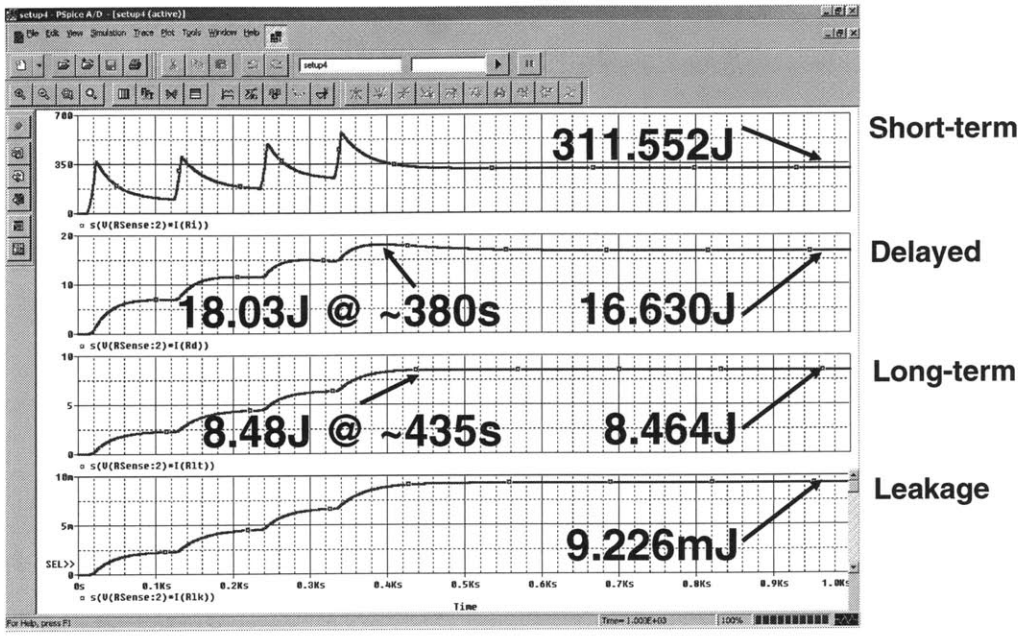

Figure 4.10: 100 A PSpice® Simulation Energy Results for each Brach

branch that contains only a resistive element. The summation of the four final energies equates to 336.66 J which is the final energy shown in Fig. 4.9.

4.6 100 A Experiment with Delay

The second experiment is very similar to the first in that both experiments charged an initially discharged device with a constant current of 100 A until the terminal voltage reached approximately 0.5 V. At this point, instead of immediately discharging the device through the resistive load, the circuit transitioned to the open-circuit mode thus allowing the charge in the device to diffuse further into the electrode; as this occurred, the terminal voltage decreased. The charge-diffusion stage was allowed to continue until the voltage reached 0.45 V at which time the circuit transitioned again, this time to the discharging mode. The device was discharged until the terminal voltage reached 0.1 V, at which point the discharge process ended and the circuit transitioned back to the constant charging mode.

For this experiment, the charging/hold/discharging process was repeated for 3 cycles; after the 3^{rd} charging/holding phase, the device was allowed to discharge through the resistive load until the end of the experiment. This particular experiment lasted 1500 s. Figure 4.15 illustrates the first 500 s of data from this experiment (the remaining 1000 s of data has

been truncated for illustrative purposes).

The experimental power data was then examined and the device energy transfer ($\frac{E_{out}}{E_{in}}$) was calculated. With a sampling rate of 10 samples per second, the Δt for this case equals 0.1 s. The energy in and energy out for each of the three cycles in this experiment, as well as the total energy in and out are:

Cycle 1: $E_{in,1}$ = 376.6 J (10.5 s < t < 22.4 s); $E_{out,1}$ = -250.3 J (56.6 s < t < 169.6 s)

Cycle 2: $E_{in,2}$ = 330.3 J (169.7 s < t < 178.8 s); $E_{out,2}$ = -253.3 J (202.1 s < t < 302.9 s)

Cycle 3: $E_{in,3}$ = 340.9 J (303.0 s < t < 312.3s); $E_{out,3}$ = -279.3 J (363.1 s < t < 1499.9 s)

$$E_{out} = E_{out,1} + E_{out,2} + E_{out,3} = 782.9 \text{ J}$$

$$E_{in} = E_{in,1} + E_{in,2} + E_{in,3} = 1047.8 \text{ J}$$

$$\eta = |\frac{E_{out}}{E_{in}}|*100 = 74.7\% \ .$$

The experimental power data was then examined and the device energy transfer was calculated. The experimental energy transfer calculated was 74.7%.

It should be noted at this time that the point of the open-circuit portion of this experiment was to demonstrate that the energy transfer would decrease due to the I^2R losses resulting from the charge diffusion through other network resistances (R_m). The switching voltage level of 0.45 V (10% decrease from the maximum voltage) was chosen for all experiments involving this "delay." For the 100 A with delay experiment, the time required for the voltage to fall from 0.5 to 0.45 V is very small (~35 s) due to the larger voltage drop associated with the ESR. But, for the experiment involving a 10 A charge with delay (to be presented next), the Δt of the delay period is much longer, due to the smaller voltage drop associated with the ESR, and the resulting energy transfer is more noticeably affected by this delay. A comparison of the energy transfer calculation for the two 100 A experiments will lead one to conclude that due to the time constants involved (see Table 4.2) and the Δt of the delay period, the decrease in energy transfer due to I^2R losses will be hardly noticeable and difficult to measure. On the other hand, one would expect that as the delay period of the experiment is increased to a value much greater than the fast time constant of the system (something on the order of the time constant of the medium branch) we would notice a more significant decrease in system energy transfer (this result is seen in the 10 A with delay experiment as the delay period is on the order of several 100 s).

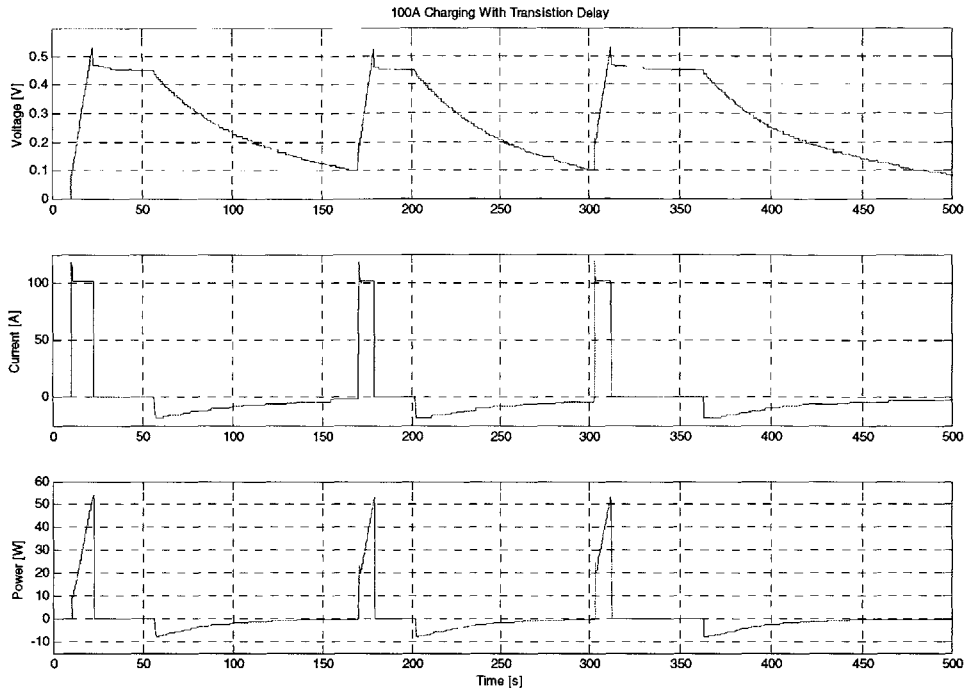

Figure 4.11: 100 A Experiment with Delay (Voltage, Current, and Power Waveforms)

4.7 100 A with Delay PSpice Simulation

A simulation based on the second current profile run in the lab was set up and run in PSpice® to help validate the DLC model developed previously and to explore the idea of using PSpice® and the DLC model to predict the performance of the actual DLC device under similar experiments.

Figure B.3 in Appendix B is a detailed diagram of the circuit set up in PSpice®. The basic circuit configuration can be seen in Fig. 4.2.

Figure 4.12 shows the resulting voltage, current, and power waveforms of this simulation. As can be seen when comparing the current waveform of Fig. 4.12 with the current waveform of Fig. 4.11, the simulation fairly accurately reproduces the experimental waveform. Furthermore, the resulting voltage waveform (and finally the power waveform) or the DLC's response to the current excitation seems to be in fair agreement with experiment.

Figure 4.13 shows the plot of energy versus time as determined when integrating the product of the voltage and current waveform with respect to time. The maximums and minimums of the plot have been labeled as these values are needed when calculating the energy transfer

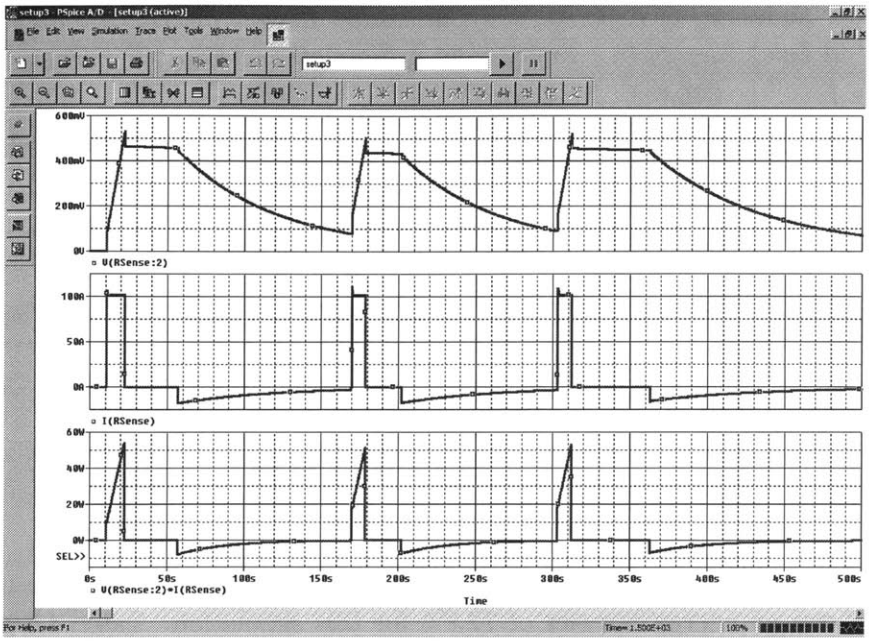

Figure 4.12: 100 A with Delay PSpice® Simulation Results (Voltage, Current, and Power Waveforms)

($\frac{E_{out}}{E_{in}}$). The energy calculation for this simulation is as follows:

$$\Delta E_n = E_{final} - E_{initial}$$

$$\Delta E_1 = 369.9 \text{ J} - 0 \text{ J} = 367.4 \text{ J} \ (10.5 \text{ s} < t < 22.4 \text{ s})$$

$$\Delta E_2 = 117.4 \text{ J} - 369.9 \text{ J} = -249.4 \text{ J} \ (56.6 \text{ s} < t < 169.6 \text{ s})$$

$$\Delta E_3 = 407.7 \text{ J} - 117.4 \text{ J} = 307.3 \text{ J} \ (169.7 \text{ s} < t < 178.8 \text{ s})$$

$$\Delta E_4 = 201.1 \text{ J} - 407.7 \text{ J} = -224.5 \text{ J} \ (202.1 \text{ s} < t < 302.9 \text{ s})$$

$$\Delta E_5 = 512.0 \text{ J} - 201.1 \text{ J} = 326.6 \text{ J} \ (303.0 \text{ s} < t < 312.3\text{s})$$

$$\Delta E_6 = 280.0 \text{ J} - 512.0 \text{ J} = -253.7 \text{ J} \ (363.1 \text{ s} < t < 1499.9 \text{ s})$$

$$E_{out} = \Delta E_2 + \Delta E_4 + \Delta E_6 = -727.6 \text{ J}$$

$$E_{in} = \Delta E_1 + \Delta E_3 + \Delta E_5 = 1001.3 \text{ J}$$

Summary of Experimental/Simulation Results for 100 A Delay Test					
Measured in Lab	*Energy In*	*Energy Out*	*Simulated in PSpice®*	*Energy In*	*Energy Out*
Cycle 1	376.6 J	-250.3 J	Cycle 1	367.4 J	-249.4 J
Cycle 2	330.3 J	-253.3 J	Cycle 2	307.3 J	-224.5 J
Cycle 3	340.9 J	-279.3 J	Cycle 3	326.6 J	-253.7 J
Total	1047.8 J	-782.9 J	Total	1001.3 J	-727.6 J
Energy Transfer	74.7%		Energy Transfer	72.7%	

Table 4.4: Summary of Experimental/Simulation Results for 100 A Delay Test

$$\eta = |\frac{E_{out}}{E_{in}}|*100 = 72.7\% \ .$$

A careful inspection of the energy delivered into the system and energy removed from the system shows an energy transfer of 72.7% for this simulation. Table 4.4 gives a detailed summary of the results of this experiment.

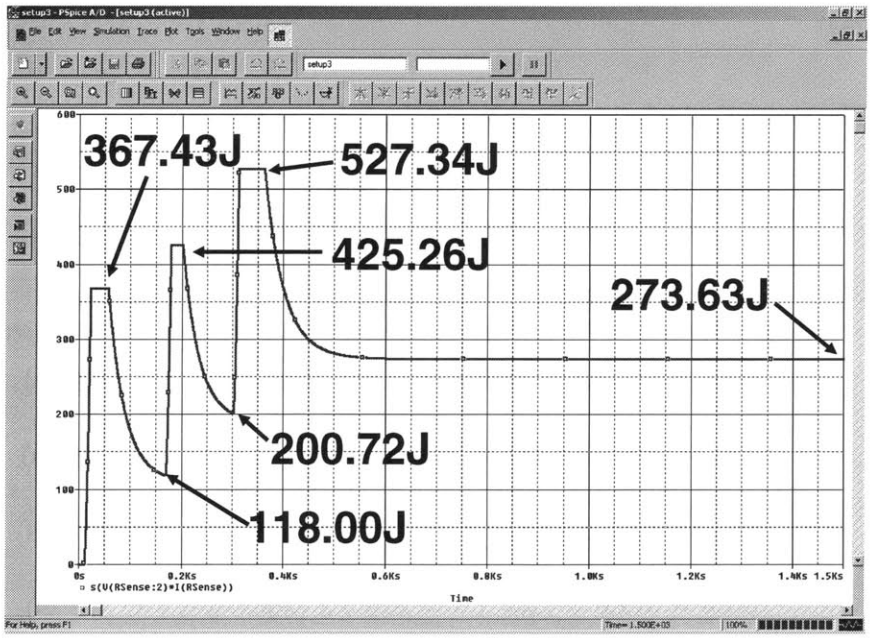

Figure 4.13: 100 A with Delay PSpice® Simulation Energy Results

An evaluation of the waveforms in Figs. 4.11, 4.12 and Table 4.4 suggests that the DLC model is able to reasonably predict (for this current profile) the terminal behavior of the actual DLC. Now, using this model we can see what is going on inside the DLC. Figure 4.14 illustrates the energy versus time waveforms for the four branches of the model presented

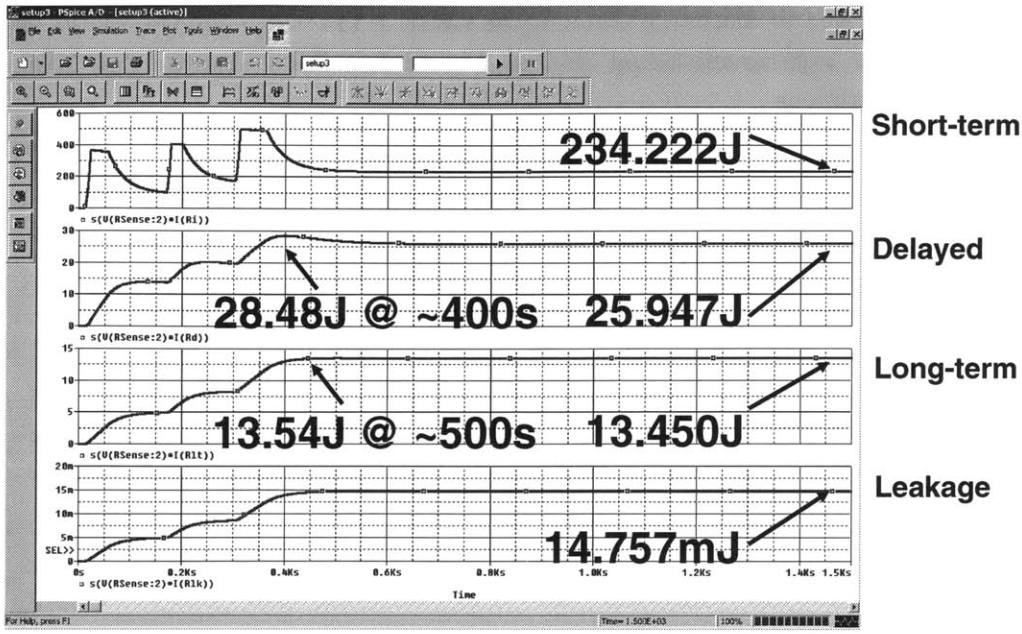

Figure 4.14: 100 A with Delay PSpice® Simulation Energy Results for each Brach

in Fig. 4.3. Looking to the second and third plot in Fig. 4.14, we can see that a maximum energy occurs at ~400 s and ~500 s respectively and then decreases to ~25.9 J and ~13.5 J respectively. This decrease in energy in the second and third plot after reaching the maximum is a result of the stored energy in the medium and slow capacitances being removed from the respective branches during the discharge of the branches. The fourth plot in Fig. 4.14 shows that the energy reaches a maximum of ~14.8 mJ and stays constant, as would be expected for a branch that contains only a resistive element. The summation of the four final energies equates to 273.63 J which is the final energy shown in Fig. 4.13.

4.8 10 A Experiment

The third experiment is nearly identical to the first except the DLC is charged with a constant current of 10 A until the voltage at the terminals reaches approximately 0.5 V. At this point in the experiment, the circuit transitions to the discharge mode; the device is discharged through a resistive load at this time until the terminal voltage reaches 0.1 V. Once the terminal voltage of the DLC reached 0.1 V, the circuit transitions back to the constant charging mode and the process begins again.

This charging/discharging process was repeated for 3 cycles; after the 3^{rd} charging phase, the

device was allowed to discharge through the resistive load until the end of the experiment. This particular experiment lasted 3000 s. Figure 4.15 illustrates the first 1000 s of data from this experiment

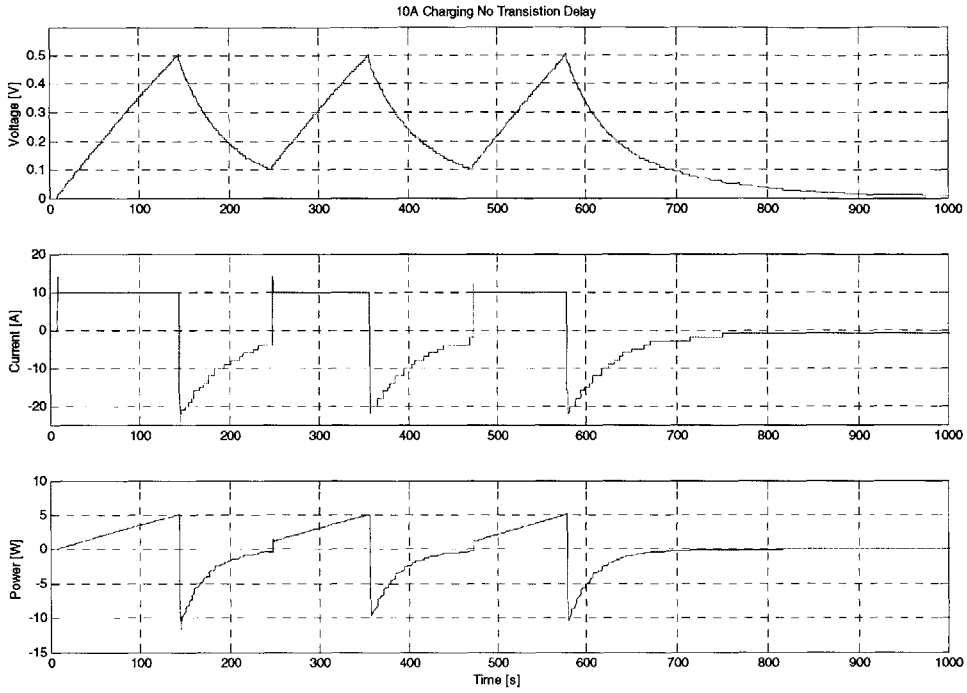

Figure 4.15: 10 A Experiment (Voltage, Current, and Power Waveforms)

The experimental power data was then examined and the device energy transfer ($\frac{E_{out}}{E_{in}}$) was calculated. With a sampling rate of 5 samples per second, the Δt for this case equals 0.2 s. The energy in and energy out for each of the three cycles in this experiment, as well as the total energy in and out are:

Cycle 1: $E_{in,1}$ = 356.4 J (9.0 s < t < 144.2 s); $E_{out,1}$ = -310.2 J (144.4 s < t < 248.2 s)

Cycle 2: $E_{in,2}$ = 332.1 J (248.4 s < t < 354.6 s); $E_{out,2}$ = -319.0 J (354.8 s < t < 472.8 s)

Cycle 3: $E_{in,3}$ = 330.1 J (473.0 s < t < 578.6 s); $E_{out,3}$ = -323.4 J (578.8 s < t < 2999.8 s)

$$E_{out} = E_{out,1} + E_{out,2} + E_{out,3} = 952.6 \text{ J}$$

$$E_{in} = E_{in,1} + E_{in,2} + E_{in,3} = 1018.6 \text{ J}$$

$$\eta = |\frac{E_{out}}{E_{in}}|*100 = 93.5\% \ .$$

The experimental power data was then examined and the device energy transfer was calculated. The experimental energy transfer calculated was 93.5%.

4.9 10 A PSpice Simulation

A simulation based on the third current profile run in the lab was set up and run in PSpice® to help validate the DLC model developed previously and to explore the idea of using PSpice® and the DLC model to predict the performance of the actual DLC device under similar experiments.

Figure B.4 in Appendix B gives the reader a detailed look at the circuit set up in PSpice®. The basic circuit configuration can be seen in Fig. 4.2.

Figure 4.16 shows the resulting voltage, current, and power waveforms of this simulation. As can be seen when comparing the current waveform of Fig. 4.16 with the current waveform of Fig. 4.15, the simulation fairly accurately reproduces the experimental waveform. Furthermore, the resulting voltage waveform (and finally the power waveform) or the DLC's response to the current excitation seems to be in fair agreement with the actual experiment.

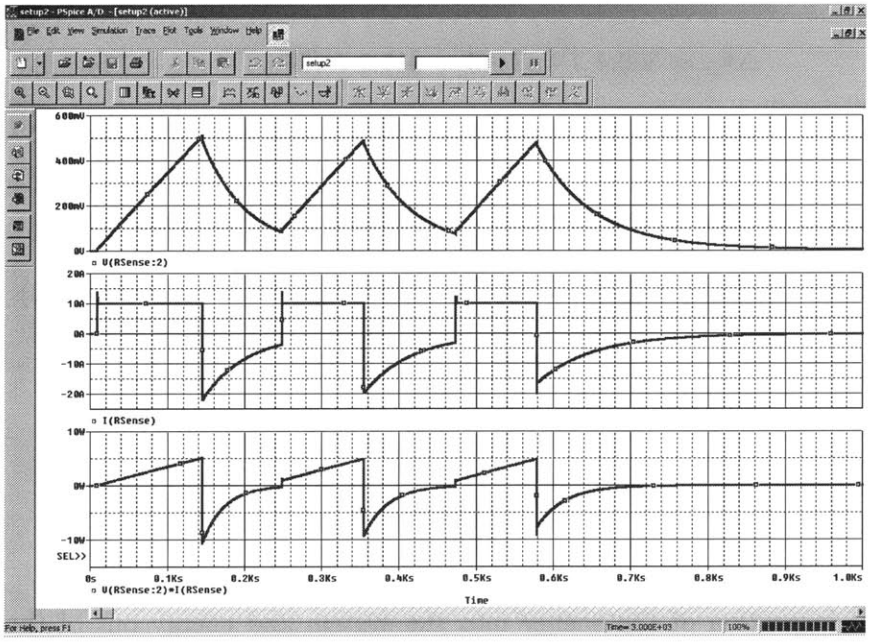

Figure 4.16: 10 A PSpice® Simulation Results (Voltage, Current, and Power Waveforms)

Figure 4.17 shows the plot of energy versus time as determined when integrating the product

Summary of Experimental/Simulation Results for 10 A Test					
Measured in Lab	*Energy In*	*Energy Out*	*Simulated in PSpice®*	*Energy In*	*Energy Out*
Cycle 1	356.4 J	-310.2 J	Cycle 1	352.3 J	-303.6 J
Cycle 2	332.1 J	-319.0 J	Cycle 2	311.1 J	-285.7 J
Cycle 3	330.1 J	-323.4 J	Cycle 3	301.0 J	-286.6 J
Total	1018.6 J	-952.5 J	Total	964.5 J	-875.9 J
Energy Transfer	93.5%		Energy Transfer	90.8%	

Table 4.5: Summary of Experimental/Simulation Results for 10 A Test

of the voltage and current waveform with respect to time. The maximums and minimums of the plot have been labeled as these values are needed when calculating the energy transfer ($\frac{E_{out}}{E_{in}}$). The energy calculation for this simulation is as follows:

$$\Delta E_n = E_{final} - E_{initial}$$

$$\Delta E_1 = 352.6 \text{ J} - 0 \text{ J} = 352.3 \text{ J} \ (9.0 \text{ s} < t < 144.2 \text{ s})$$

$$\Delta E_2 = 47.9 \text{ J} - 352.6 \text{ J} = -303.6 \text{ J} \ (144.4 \text{ s} < t < 248.2 \text{ s})$$

$$\Delta E_3 = 350.4 \text{ J} - 47.9 \text{ J} = 311.1 \text{ J} \ (248.4 \text{ s} < t < 354.6 \text{ s})$$

$$\Delta E_4 = 72.6 \text{ J} - 350.4 \text{ J} = -285.7 \text{ J} \ (354.8 \text{ s} < t < 472.8 \text{ s})$$

$$\Delta E_5 = 357.0 \text{ J} - 72.6 \text{ J} = 301.0 \text{ J} \ (473.0 \text{ s} < t < 578.6 \text{ s})$$

$$\Delta E_6 = 90.5 \text{ J} - 357.0 \text{ J} = -286.6 \text{ J} \ (578.8 \text{ s} < t < 2999.8 \text{ s})$$

$$E_{out} = \Delta E_2 + \Delta E_4 + \Delta E_6 = -875.9 \text{ J}$$

$$E_{in} = \Delta E_1 + \Delta E_3 + \Delta E_5 = 964.4 \text{ J}$$

$$\eta = |\frac{E_{out}}{E_{in}}| * 100 = 90.8\% \ .$$

A careful inspection of the energy into the system and energy out of the system shows an approximate energy transfer for this simulation. The energy transfer found for this simulation was 90.8%. Table 4.5 gives a detailed summary of the results of this experiment.

An evaluation of the waveforms in Figs. 4.15, 4.16 and Table 4.5 suggests that the DLC

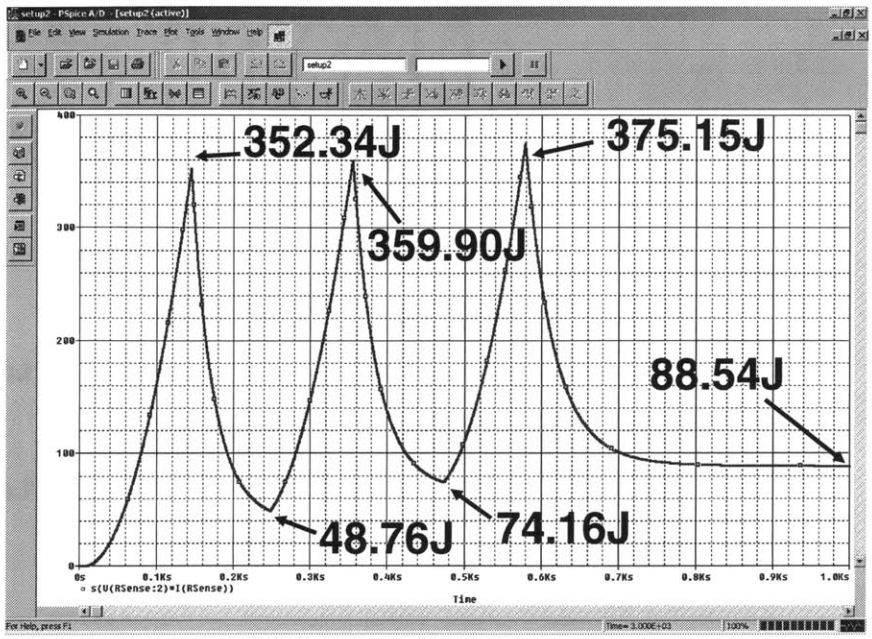

Figure 4.17: 10 A PSpice® Simulation Energy Results

model is able to reasonably predict (for this current profile) the terminal behavior of the actual DLC. Now, using this model we can see what is going on inside the DLC. Figure 4.18 illustrates the energy versus time waveforms for the four branches of the model presented in Fig. 4.3. Looking to the second and third plot in Fig. 4.18, we can see that a maximum energy occurs at ~620 s and ~735 s respectively and then decreases to ~25.3 J and ~15.6 J respectively. This decrease in energy in the second and third plot after reaching the maximum is a result of the stored energy in the medium and slow capacitances being removed from the respective branches during the discharge of the branches. The fourth plot in Fig. 4.18 shows that the energy reaches a maximum of ~18.0 mJ and stays constant, as would be expected for a branch that contains only a resistive element. The summation of the four final energies equates to 88.54 J which is the final energy shown in Fig. 4.17.

4.10 10 A Experiment with Delay

The fourth experiment is very similar to the second except that the device was charged with a constant current of 10 A until the terminal voltage reached approximately 0.5 V. At this point the circuit transitioned to the open-circuit mode thus allowing the charge in the device to diffuse further into the network. The charge-diffusion stage was allowed to continue until the voltage reached 0.45 V at which time the circuit transitioned again, this

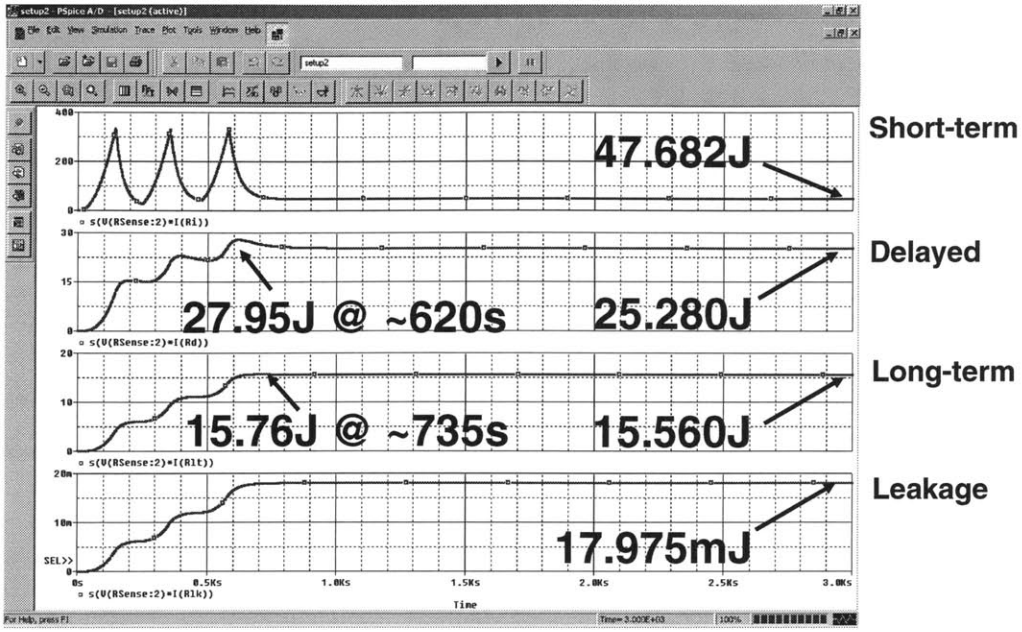

Figure 4.18: 10 A PSpice® Simulation Energy Results for each Brach

time to the discharging mode as mentioned above. The device was allowed to discharge at this time for the remainder of the experiment.

This process was performed for 1 cycle; the device was then allowed to discharge through the resistive load until the end of the experiment. This particular experiment lasted 3000 s. Figure 4.19 illustrates the data from this experiment.

The experimental power data was then examined and the device energy transfer ($\frac{E_{out}}{E_{in}}$) was calculated. With a sampling rate of 5 samples per second, the Δt for this case equals 0.2 s. The energy in and energy out for the single cycle of this experiment, as well as the total energy in and out are:

Cycle 1: $E_{in,1}$ = 355.4 J (9.8 s < t < 144.8 s); $E_{out,1}$ = -275.1 J (537.2 s < t < 2999.8 s)

$$E_{out} = E_{out,1} = \text{-}275.1 \text{ J}$$

$$E_{in} = E_{in,1} = 355.4 \text{ J}$$

$$\eta = |\frac{E_{out}}{E_{in}}|*100 = 77.4\% \ .$$

The experimental power data was then examined and the device energy transfer was calcu-

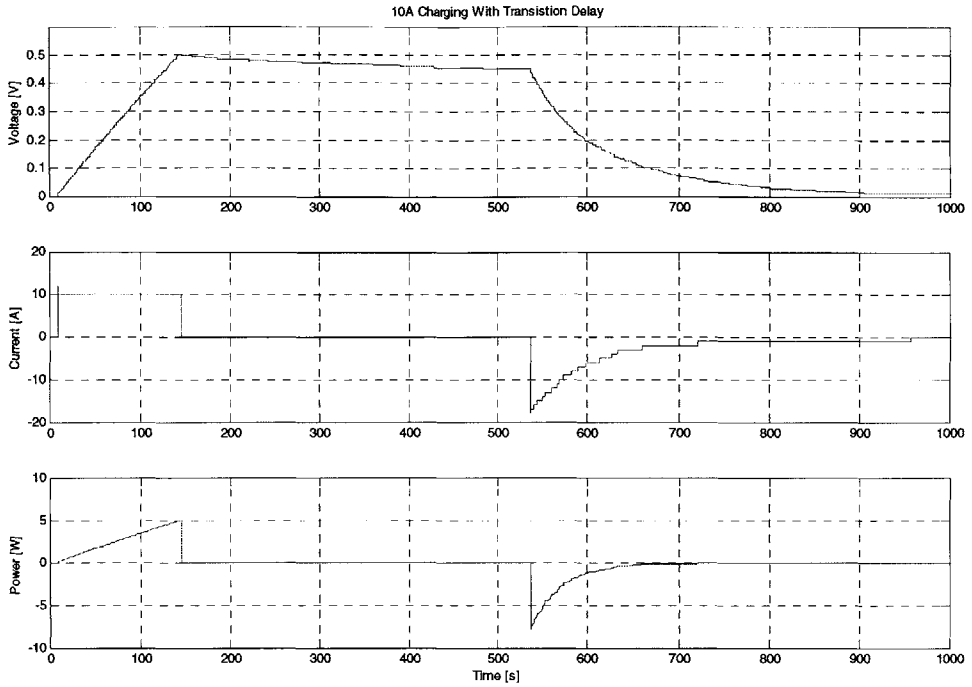

Figure 4.19: 10 A Experiment with Delay (Voltage, Current, and Power Waveforms)

lated. The experimental energy transfer calculated was 77.4%.

The results of this experiment should now be considered as compared to the 10 A (no delay) experiment. In both 10 A experiments, the device received the same charging current for approximately the same time period. The only main difference between the two 10 A experiments was that in the 10 A with delay experiment, the charge was allowed to diffuse further into the electrode, thus incurring additional I^2R losses as the charge diffused and as the charge was removed from the device during the discharge phase. The Δt period for the delay is $\sim$400 s (comparable to the medium time constant). Thus as mentioned before, this is a case where the decrease in energy transfer due to this loss mechanism is appreciable.

4.11 10 A with Delay PSpice Simulation Simulation

A simulation based on the fourth current profile run in the lab was set up and run in PSpice® to help validate the DLC model developed previously and to explore the idea of using PSpice® and the DLC model to predict the performance of the actual DLC device under similar experiments.

Figure B.5 in Appendix B gives the reader a detailed look at the circuit set up in PSpice®. The basic circuit configuration can be seen in Fig. 4.2.

Figure 4.20 shows the resulting voltage, current, and power waveforms of this simulation. As can be seen when comparing the current waveform of Fig 4.20 with the current waveform of Fig. 4.19, the simulation fairly accurately reproduces the experimental waveform. Furthermore, the resulting voltage waveform (and finally the power waveform) or the DLC's response to the current excitation seems to be in fair agreement with experiment.

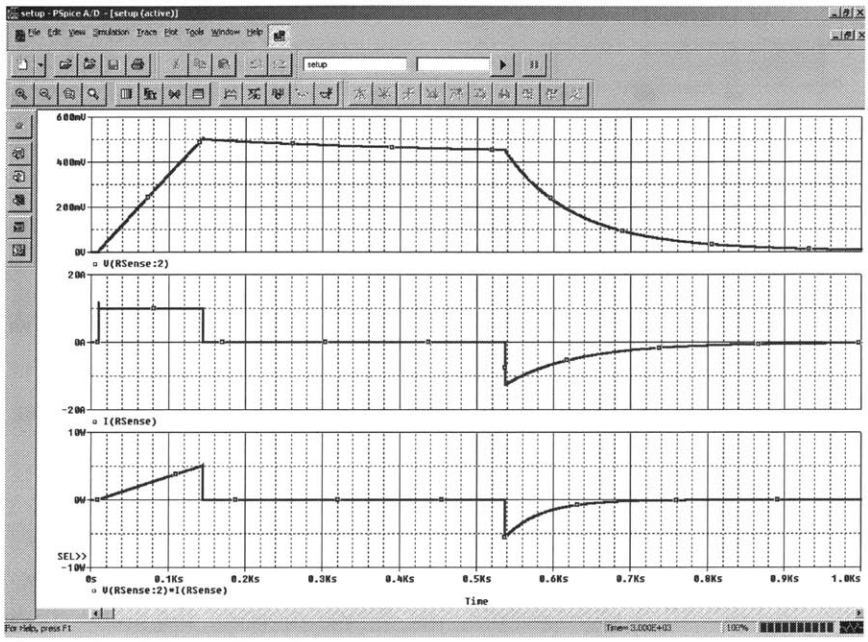

Figure 4.20: 10 A with Delay PSpice® Simulation Results (Voltage, Current, and Power Waveforms)

Figure 4.21 shows the plot of energy versus time as determined when integrating the product of the voltage and current waveform with respect to time. The maximums and minimums of the plot have been labeled as these values are needed when calculating the energy transfer ($\frac{E_{out}}{E_{in}}$). The energy calculation for this simulation is as follows:

$$\Delta E_n = E_{final} - E_{initial}$$

$$\Delta E_1 = 351.1 \text{ J} - 0 \text{ J} = 350.9 \text{ J} \ (9.8 \text{ s} < t < 144.8 \text{ s})$$

$$\Delta E_2 = 83.8 \text{ J} - 351.1 \text{ J} = -268.8 \text{ J} \ (537.2 \text{ s} < t < 2999.8 \text{ s})$$

$$E_{out} = \Delta E_2 = -268.8 \text{ J}$$

Summary of Experimental/Simulation Results for 10 A Delay Test					
Measured in Lab	*Energy In*	*Energy Out*	*Simulated in PSpice®*	*Energy In*	*Energy Out*
Cycle 1	355.4 J	-275.1 J	Cycle 1	350.9 J	-268.8 J
Total	355.4 J	-275.1 J	Total	350.9 J	-268.8 J
Energy Transfer	77.4%		Energy Transfer	76.6%	

Table 4.6: Summary of Experimental/Simulation Results for 10 A Delay Test

$$E_{in} = \Delta E_1 = 350.9 \text{ J}$$

$$\eta = |\frac{E_{out}}{E_{in}}|*100 = 76.6\% \ .$$

A careful inspection of the energy delivered into the system and energy removed from the system shows an energy transfer of 76.6% for this simulation. Table 4.6 gives a detailed summary of the results of this experiment.

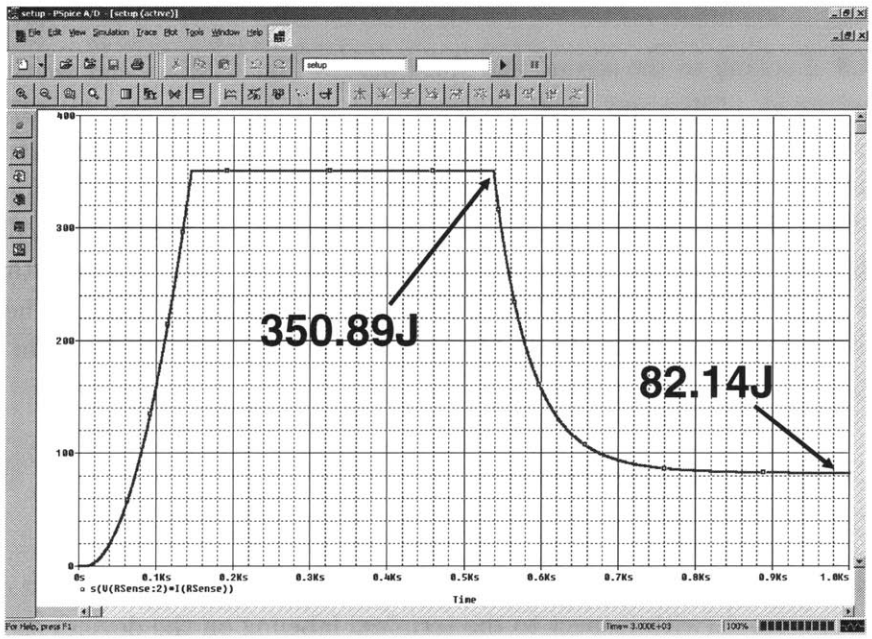

Figure 4.21: 10 A with Delay PSpice® Simulation Energy Results

An evaluation of the waveforms in Figs. 4.19, 4.20 and Table 4.6 suggests that the DLC model is able to reasonably predict (for this current profile) the terminal behavior of the actual DLC. Now, using this model we can see what is going on inside the DLC. Figure 4.22 illustrates the energy versus time waveforms for the four branches of the model presented

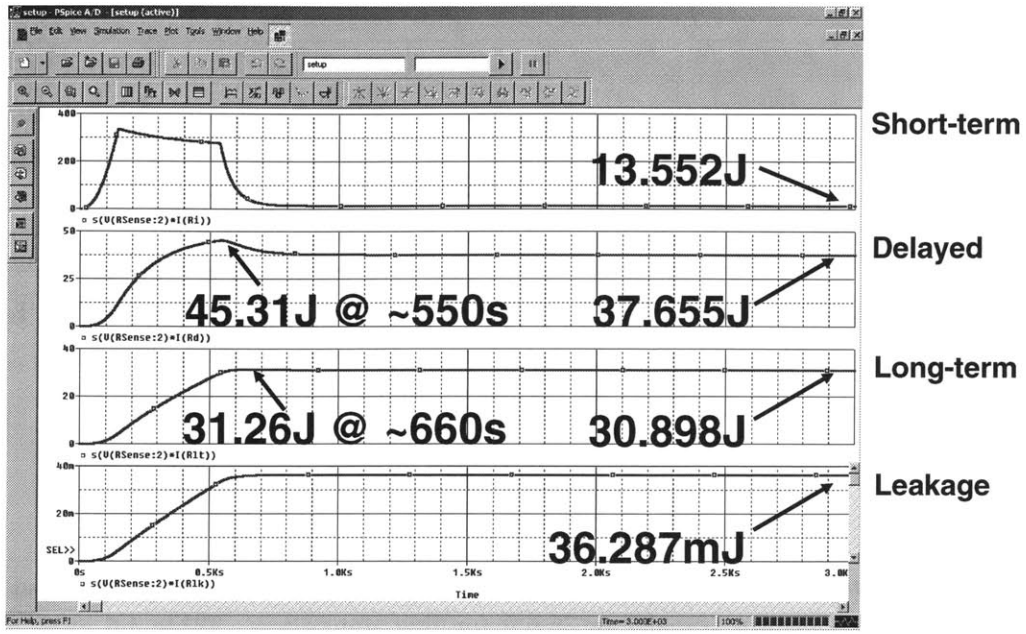

Figure 4.22: 10 A with Delay PSpice® Simulation Energy Results for each Branch

in Fig. 4.3. Looking to the second and third plot in Fig. 4.22, we can see that a maximum energy occurs at ~550 s and ~660 s respectively and then decreases to ~37.7 J and ~30.9 J respectively. This decrease in energy in the second and third plot after reaching the maximum is a result of the stored energy in the medium and slow capacitances being removed from the respective branches during the discharge of the branches. The fourth plot in Fig. 4.22 shows that the energy reaches a maximum of ~36.3 mJ and stays constant, as would be expected for a branch that contains only a resistive element. The summation of the four final energies equates to 82.14 J which is the final energy shown in Fig. 4.21.

4.12 -100 A Experiment

The final experiment performed in the laboratory is very similar to the first except that the device was reversed (with respect to the terminal labeling on the device) on the test circuit before being charged with a constant current of 100 A. The device received this constant charge until the terminal voltage reached approximately -0.5 V. At this point the circuit transitioned to the discharging mode as mentioned above in a similar fashion to the 100 A (no delay) test. The device was then discharged through the resistive load until the terminal voltage reached 0.1 V. Once the terminal voltage of the DLC reached 0.1 V, the constant charging process began again.

This charging/discharging process was repeated for 3 cycles; after the 3^{rd} charging phase, the device was allowed to discharge through the resistive load until the end of the experiment. This particular experiment lasted 1000 s. Figure 4.23 illustrates the first 500 s of data from this experiment.

With a sampling rate of 5 samples per second, the Δt for this case = 0.2 s. The energy in and energy out for each of the three cycles in this experiment, as well as the total energy in and out are:

Cycle 1: $E_{in,1}$ = -373.4 J (9.1 s < t < 21.3 s); $E_{out,1}$ = 273.7 J (21.5 s < t < 130.1 s)

Cycle 2: $E_{in,2}$ = -351.3 J (130.3 s < t < 140.1 s); $E_{out,2}$ = 292.3 J (140.3 s < t < 241.5 s)

Cycle 3: $E_{in,3}$ = -344.3 J (241.7 s < t < 251.3 s); $E_{out,3}$ = 298.6 J (251.5 s < t < 999.9 s)

$$E_{out} = E_{out,1} + E_{out,2} + E_{out,3} = 864.6 \text{ J}$$

$$E_{in} = E_{in,1} + E_{in,2} + E_{in,3} = 1069.0 \text{ J}$$

$$\eta = |\frac{E_{out}}{E_{in}}|*100 = 80.9\% \ .$$

The experimental power data was then examined and the device energy transfer was calculated. The experimental energy transfer calculated was 80.9%.

The energy transfer of this experiment was expected to be very close to that of the first experiment (100 A no delay), but what was found was that the energy transfer measured was noticeably higher. Is this contradiction to the assumed energy transfer a product of experimental error? If not, what could cause this observed phenomenon?

4.13 Summary of Experimental/Simulation Results

With the exception of the final experiment, the experimental results seem pretty much inline with expectation and simulation. The results of the experiment presented in Section 4.12 indicate a non-symmetrical design of the device.

Table 4.7 shows a summary of the energy transfer for the experiments covered in this chapter. As can be seen for this table, the model (shown in Fig. 4.3) is able to predict the performance of the device when the device's polarity marking are properly observed, but

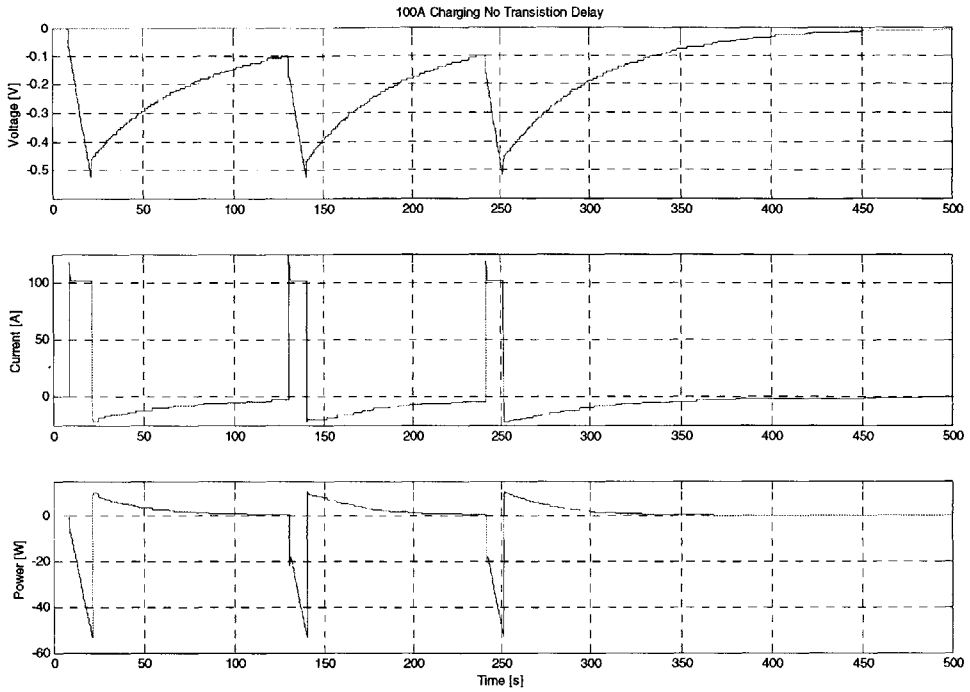

Figure 4.23: -100 A Experiment (Voltage, Current, and Power Waveforms)

Summary of Experimental/Simulation Results					
	100 A No Delay	*100 A With Delay*	*10 A No Delay*	*10 A With Delay*	*-100 A No Delay*
Cycles	4	3	3	1	3
Experimental $\eta(\%)$	74.7	74.7	93.5	77.4	80.9
PSpice® $\eta(\%)$	74.7	72.7	90.8	76.6	N/A

Table 4.7: Summary of Experimental/Simulation Results

the model is unable to predict the performance of the device when the polarity is reversed. Table 4.8 gives a summary of the simulated energy losses in each of the individual branches. These results of the simulation show that the higher current experiments incurred higher energy losses in the fast branch than the lower current experiments. Additionally, the delay experiments show a higher loss in the medium and slow branches than the non-delay experiments for the same charging current. Finally, the longer duration experiments show a larger energy loss for the leakage resistor branch.

Experiment	*Summary of Simulated Branch Energy Losses*				
	Fast Branch	*Delay Branch*	*Slow Branch*	*Leakage Resistor*	*Duration of Experiment*
100 A No Delay	311.552 J	16.630 J	8.464 J	9.226 mJ	1000 s
100 A With Delay	234.222 J	25.947 J	13.450 J	14.757 mJ	1500 s
10 A No Delay	47.682 J	25.280 J	15.560 J	17.975 mJ	3000 s
10 A With Delay	13.552 J	37.655 J	30.898 J	36.287 mJ	3000 s

Table 4.8: Summary of Simulated Branch Energy Losses

Chapter 5

Temperature Effects on DLCs

5.1 Introduction

Energy storage devices used in automotive type applications are likely to be subjected to a variety of environments in the course of the vehicle's/application's lifetime. The temperature of the environment in which the device is used is one such consideration. This chapter will investigate, and present information on, the temperature trends as they are relevant to DLCs. The desire was to investigate what effects low/high temperatures have on DLCs. To do so, three experiments were scheduled: 1) a room temperature "base-line" experiment, 2) a high temperature experiment, and 3) a low temperature experiment. An experimental setup was designed/constructed, one which would allow all three experiments to be performed without breaking-down and reconstructing the experimental setup between the experiments. With the experimental setup constructed, the room temperature experiment was performed. Next, the device was thoroughly discharged ("reset") and the high temperature experiment performed. Finally, the device was reset again and the low temperature experiment performed.

A diagram of the experimental setup is shown in Fig. 5.1. The device used is a 2500 F Nesscap DLC. Copper foil was placed in the terminals of the device before stainless steel lugs were screwed into place. A coaxial cable was soldered to the copper foil and hooked to a TDS 745D oscilloscope. This connection provided the measurement of the devices terminal voltage. Brass bolts were then placed on the device to hold the copper ring-connects (which were connected to 2 AWG wire that provided the charging current to the device). The current source was a HP 6011A set to provide ~100 A. An A6303 current probe (gun type) was connected to an AM 503 current amplifier which was used to measure the charging current. The current amplified was also connected to the oscilloscope where the data was collected and stored during the experiment. A Fluke multimeter (not shown in Fig. 5.1), set as a voltage meter, was used to observe the rising voltage as the device was charged. The final components of the test setup are a low-impedance resistive load (for discharging the device) and a three position mechanical switch. The three position switch allowed the device to be charged via the current source, open-circuited, or discharged through the

resistive load.

One of the goals of this exercise was to carefully perform three experiments, and to do so while eliminating as many unnecessary variables as possible. All three experiments started with a thoroughly discharged device, were charged with the current source set at 100 A for a time period such that device's terminal voltage read ~0.5 V, and then open circuited for the remainder of the experiment. Each experiment collected data for 3000 s. From the voltage and current information collected during each experiment, DLC models were derived by the methods presented in Chapter 3. Fig. 5.2 shows the DLC model that the data was fitted to.

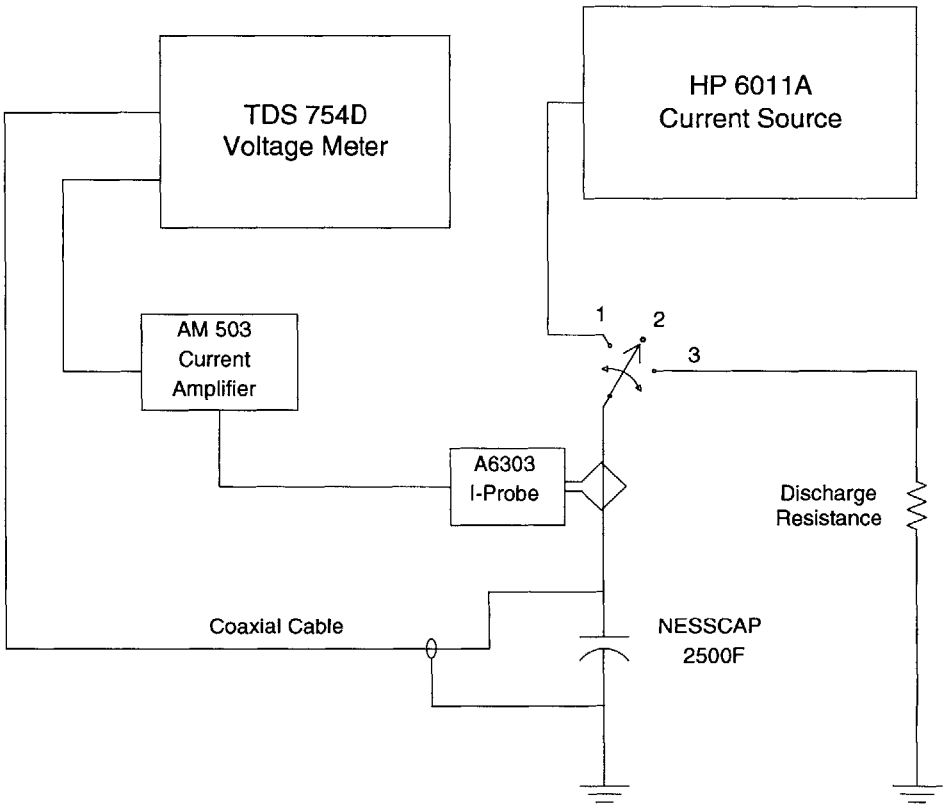

Figure 5.1: Basic Experimental Test Circuit

5.2 Room Temperature Experiment

The first experiment in this series of three experiments is the room temperature experiment. The room temperature experiment was performed to establish a "base-line" DLC model for the device under test (DUT). Its results will be used in a comparison of the device's

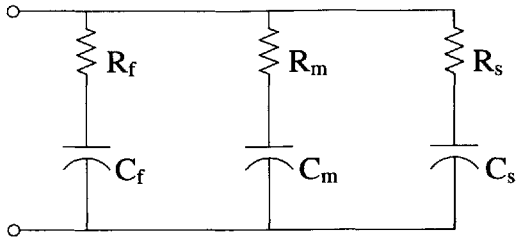

Figure 5.2: Basic DLC Model

performance under other temperature environments.

5.2.1 Test Setup

The test setup used in this experiment is the most basic of the three experiments. Figure 5.1 gives a block diagram of the setup. The DUT was placed inside the CENCO oven and connected to the circuit. The device needed to be in the oven for the high temperature experiment, therefore the room temperature test was performed with the device in the oven, but with the oven off and the door of the oven open. An illustration of the oven, the current probe, and a portion of the test setup can be seen in Fig. 5.3. Figure 5.4 gives a detailed look at the side of the oven. From Fig. 5.4, several important details of the setup can be seen. A group of wires can be seen entering the side of the oven (near the door latch). Within this group of wires are the positive and negative wires used to charge the DLC, coaxial cable connected to the terminals of the DLC (for voltage measurements recordable by the oscilloscope), the oven's thermocouple (used by the oven's controller), a thermocouple connected to a Cole Parmer® Digi-Sense® thermometer (used to observe the encloser's temperature by the user), and a pair of wires connected to the terminals of the DLC to give voltage reading to the Fluke multimeter (used to observe the device's voltage by the user) seen in Fig. 5.3.

One final detail of Fig. 5.4 will be mentioned at this time. A clear tube can be seen entering the side of the oven (below the bundle of wires). This tube was used to inject nitrogen gas into the enclosure during the high temperature experiment. The nitrogen gas was not used for either the room temperature experiment or the low temperature experiment. The tube was left in place during all three experiments.

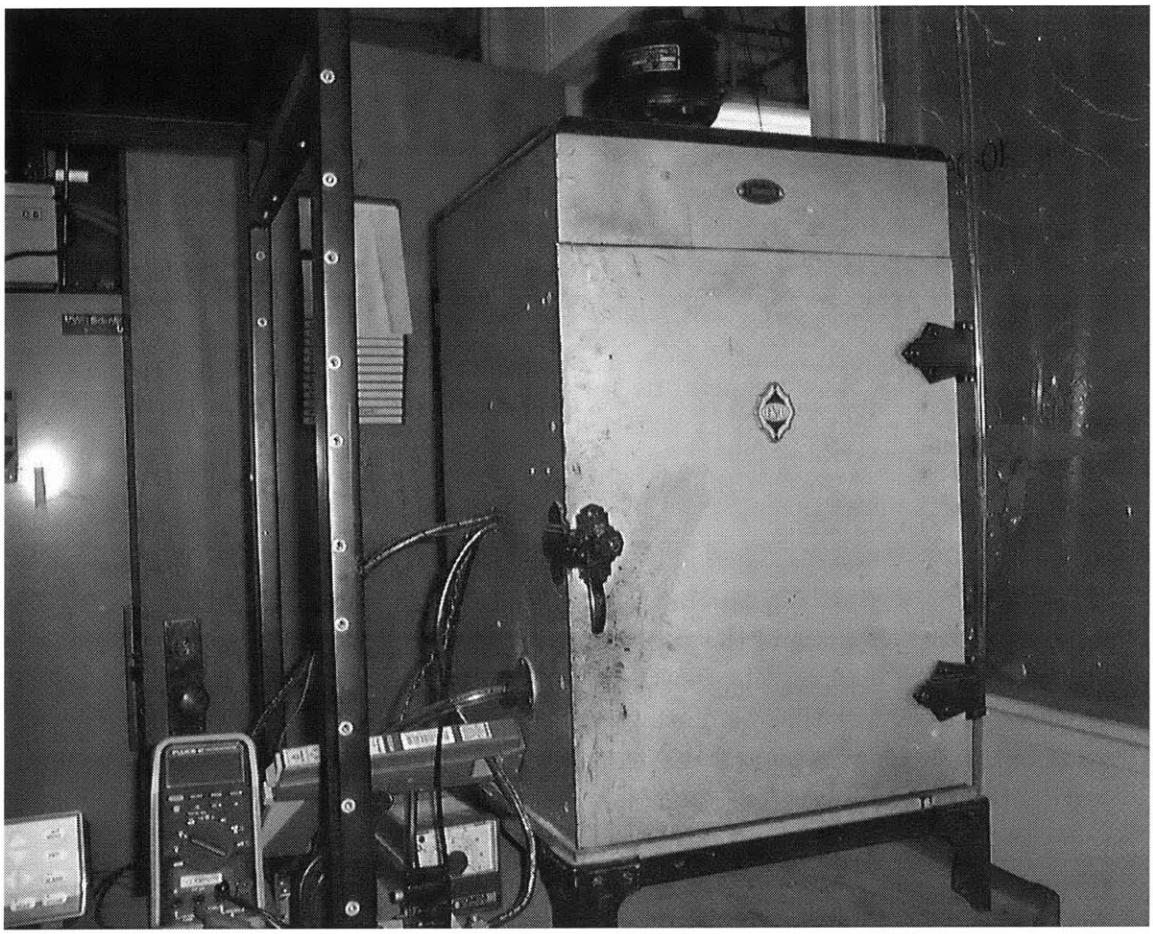

Figure 5.3: Oven Test Setup

5.2.2 Results

Once the device was connected to the test setup, the device was charged to ~0.5 V by a constant current. The voltage and current measurements were collected by the oscilloscope and the information examined after the test. Using the data collected during the test and the modeling procedure outlined in Chapter 3, a DLC model was extracted for the room temperature experiment. Figure 5.6 illustrates the room temperature circuit model derived for this device. Table 5.1 summarizes the room temperature parameters of the model as well as the time constants.

Using the Simulink™/Matlab® method of simulating the DLC model and comparing the experimental results, as presented in Chapter 3, Figs. 5.7 - 5.9 have been generated.

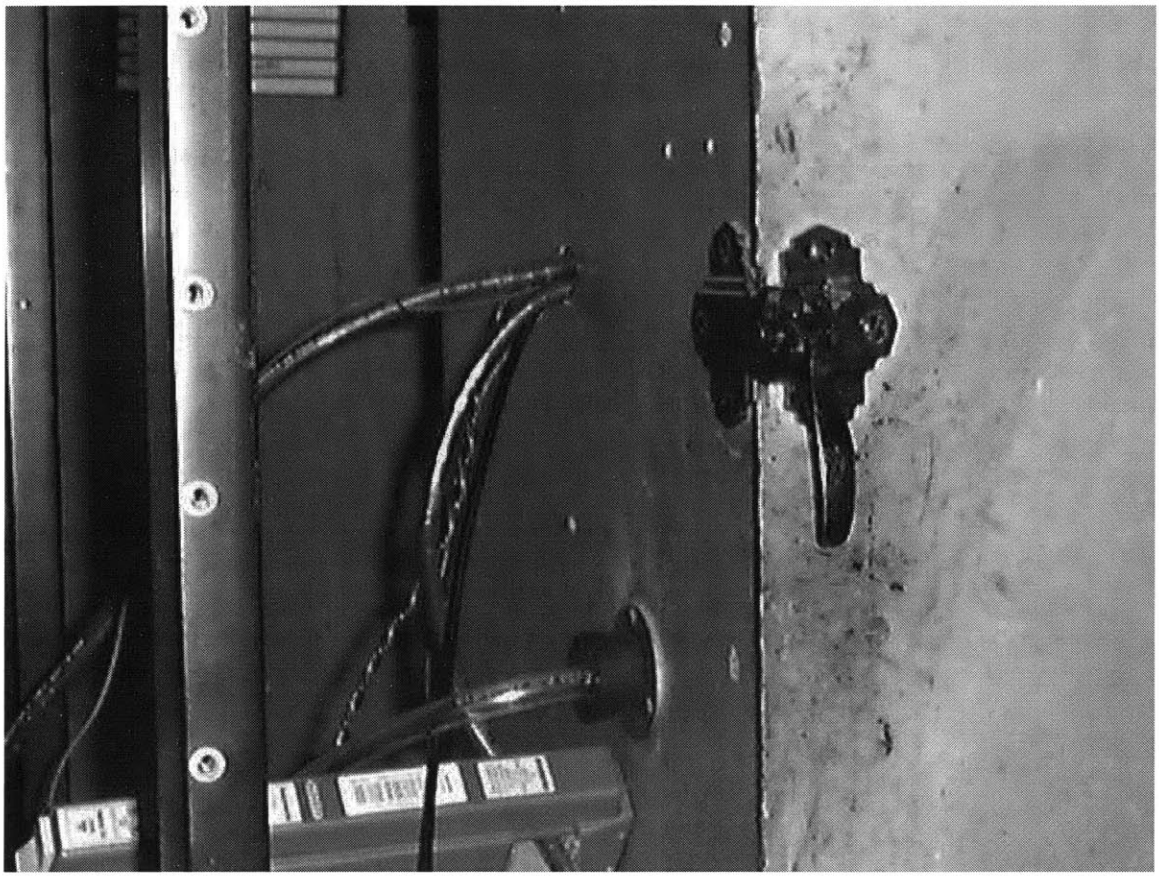

Figure 5.4: Wires and Gas Line Entering Oven

Figure 5.7 illustrates the device's and model's performance from 0 to 30 s. As can be seen from this figure, the performance of the model tracks the performance of the device very well. Both curves demonstrate an initial jump in voltage when the current source is applied to the device and model, and a linear rise in voltage to ~0.5 V. The values (voltage) of both curves drop once the current source is removed and continues to slowly decrease in time.

Looking on the time scale of 0 to 300 s (Fig. 5.8), the performance of the model is very good when compared to the performance of the device. Both curves are in very good agreement as the voltage decreases.

Figure 5.9 shows the performance of the model and device from 0 to 3000 s. The model shows fair agreement with the performance of the device.

Figure 5.5: DLC in Oven

5.3 High Temperature Experiment

With the room temperature experiment completed, the DUT was thoroughly discharged (via a copper shorting bar) in preparation for the high temperature experiment. The goal of the high temperature experiment was to look at what effects a high temperature environment would have on the performance of the DLC. In order to understand this, a high temperature DLC model would need to be determined so that it can be compared to the DLC model found at room temperature.

5.3.1 Test Setup

The test setup for this experiment is essentially the same at the ones used for the room temperature experiment. None of the connections to the DUT were disturbed since the setup had been constructed. The discharging of the DUT (in preparation for the next

	NessCap 2500 F DLC		
	Resistance (Ω)	*Capacitance* (Farad)	*Time Constant* (second)
Fast	0.000508	2641	1.34
Medium	0.04562	148.1	6.8
Slow	0.988	618.5	611

Table 5.1: Extracted Parameters for the 2500 F NessCap DLC Model (Room Temperature)

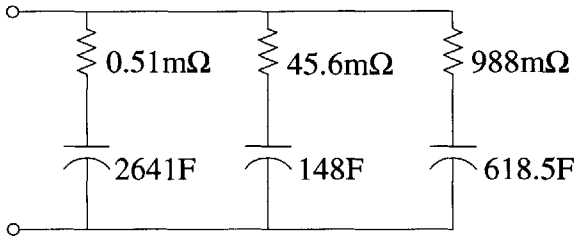

Figure 5.6: Extracted Room Temperature Model for 2500 F NessCap DLC

experiment) through the resistive load was performed using the mechanical switch shown in Fig. 5.1. Additionally, once the device voltage reached ~0 V, the device was short circuited with a copper shorting bar to provide a low impedance discharge path for the duration between experiments. The setup is constructed such that the copper bar can be placed on the device and removed without disturbing the electrical connections.

There are two significant differences between the room temperature experiment and the high temperature experiment that should be mentioned. The first is the temperature of the environment. The goal was to expose the DUT to a higher temperature environment (for an extended period of time so that the device's temperature may approximately reach the temperature of the environment) in order to investigate the quantitative temperature trends of the device. The oven was set to operate at ~50 °C. Figure 5.10 illustrates a plot of the measured temperature with time. The thermocouple used to measure the temperature was placed on the top of the device, in contact with its aluminum casing. The oven reached ~52 °C and was held there for at least 2 hours before the experiment began. It will be noticed in Fig. 5.10 that the oven was turned off at the beginning of the experiment and that the temperature declined slightly during the 50 minute experiment to ~47 °C. It was noticed that as the oven switched on and off to hold the temperature at ~52 °C the oscilloscope picked up a large amount of switching noise. It was decided that rather than attempt to suppress the noise from the measurements while having the oven on, the solution of turning off the oven during the quick experiment would be acceptable. This study did not set out to qualitatively map the temperature characteristics of the DLC, but rather to

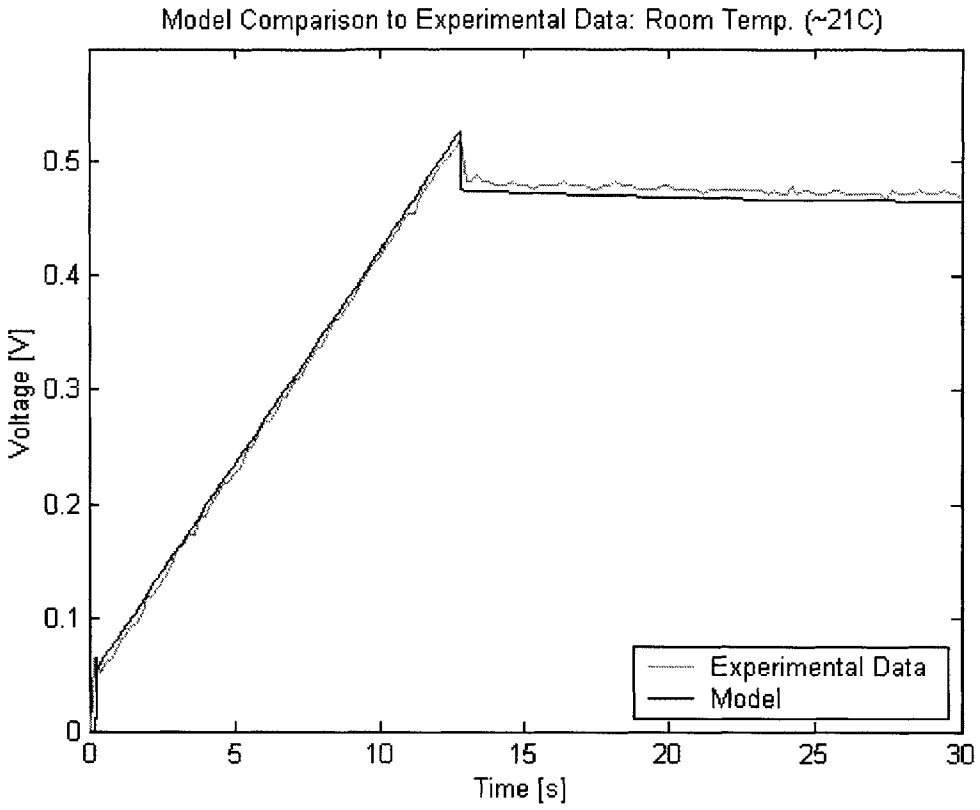

Figure 5.7: Room Temperature Model Comparison for 2500 F NessCap DLC (0 to 30 s)

quantitatively investigate them. The solution of turning off the oven did not hinder the study's goal.

The second difference in this setup was the use of nitrogen gas within the oven. The nitrogen gas was used as a safety measure for this experiment. The concern (although very unlikely) was that the device might catch fire and release toxins into the laboratory. The nitrogen was pumped into the oven, which reduced the amount of oxygen available in the enclosure, thus reducing the chances of fire.

5.3.2 Results

The high temperature experiment was performed using the "modeling" profile as the previous experiment. For this experiments, the initially discharged device received a pulse of constant current until the device voltage reached ~0.5 V. The current source was then

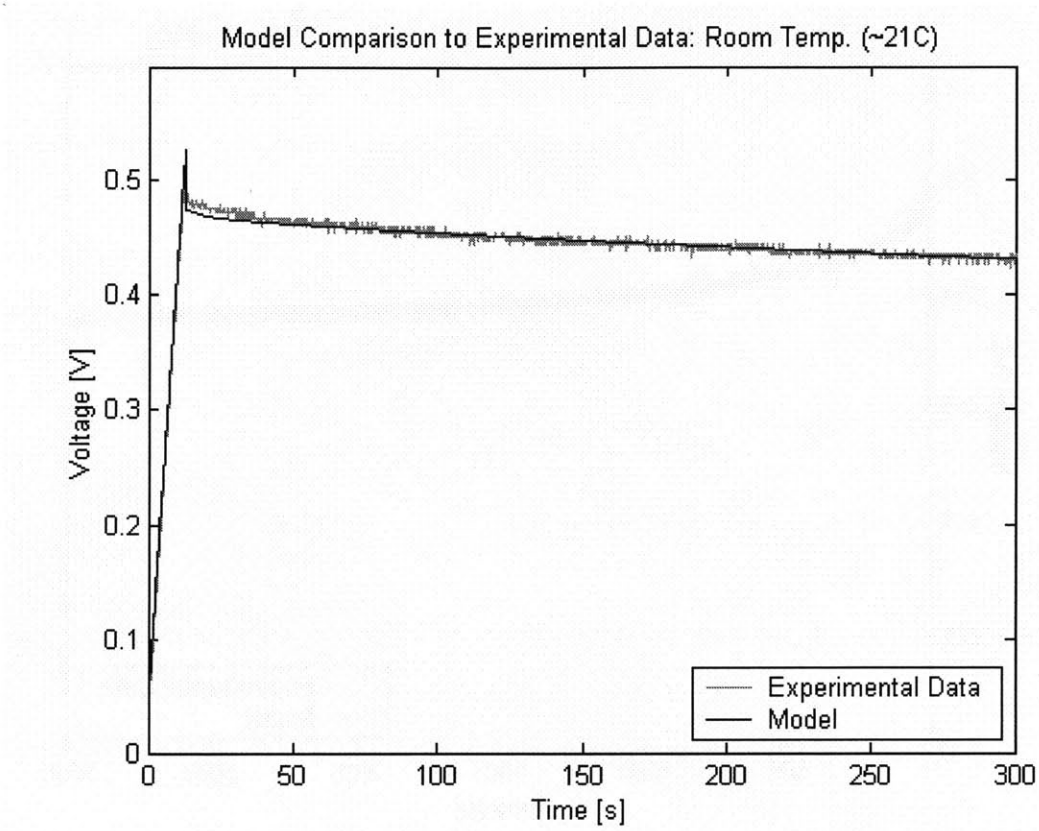

Figure 5.8: Room Temperature Model Comparison for 2500 F NessCap DLC (0 to 300 s)

removed and the device open circuited for the remainder of the experiment. With the experiment complete, the data was collected, examined, and a high temperature DLC model derived using the modeling procedure documented in Chapter 3. Figure 5.11 illustrates the derived circuit model for this device under elevated temperatures. The parameters of the circuit as well as the branch time constants are summarized in Table 5.2.

Once the high temperature model was determined, the model was constructed in the Simulink™/Matlab® program mentioned previously. The results of the simulation/ comparison are shown in Figs. 5.12 - 5.14. Figure 5.12 illustrated the first 30 s of the experiment. The experimental data is seen to have an initial jump at the beginning of the experiment, followed by a nearly linear rise to ~0.5 V. The data curve then peaks around 13 s, has an abrupt fall in voltage (once the current source is removed), and decreases for the remainder of the plot. The model can be seen plotted against the experimental data and proves to provide a fair fit.

Figure 5.13 shows the experimental/simulation information for the first 300 s for the high

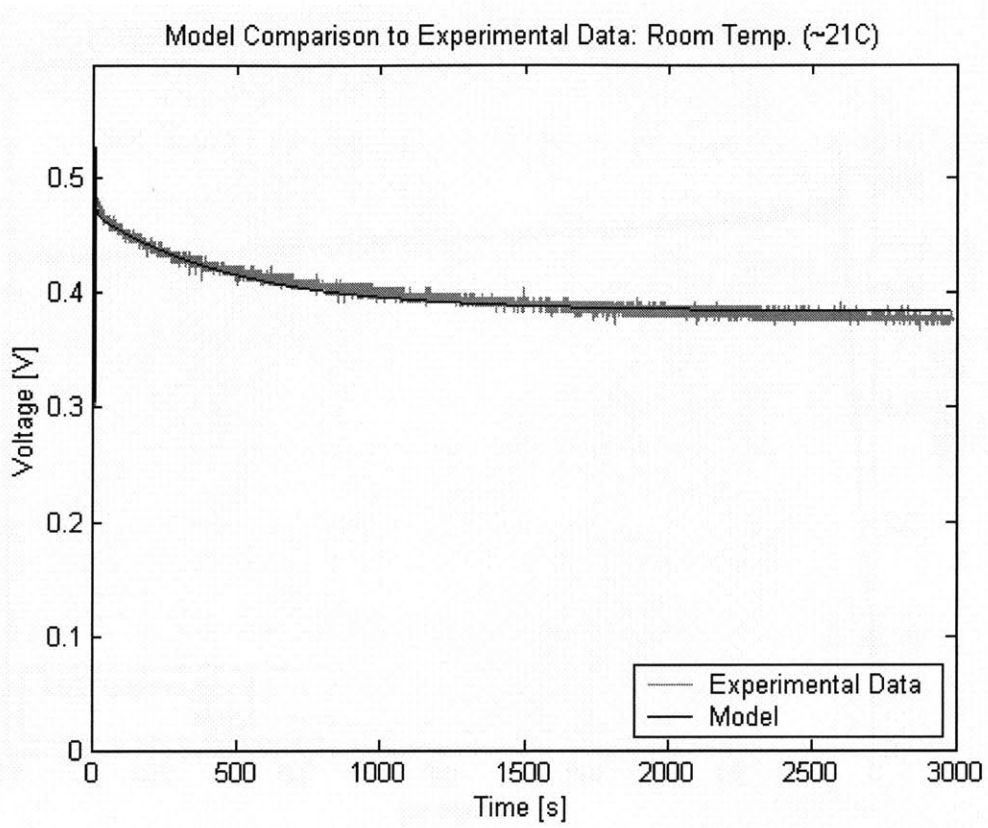

Figure 5.9: Room Temperature Model Comparison for 2500 F NessCap DLC (0 to 3000 s)

temperature comparison. Figure 5.14 illustrates the entire experiment from 0 to 3000 s. The model can be seen in Figs. 5.13 & 5.14 to provide a good fit.

5.4 Low Temperature Experiment

The final experiment in the study of the temperature trends of DLCs was the low temperature experiment. Energy storage devices used in automotive applications are often subjected to low temperature environments. The stresses that a low temperature environment has on automotive batteries can easily lead to system failure. It is important to understand the effects of low temperature on DLCs as DLCs may be used in conjunction with batteries in an advanced automotive electrical system. In an effort to understand the device's low temperature characteristics, a low temperature experiment was desired. With the information gathered from such an experiment, a low temperature model could be extracted and examined.

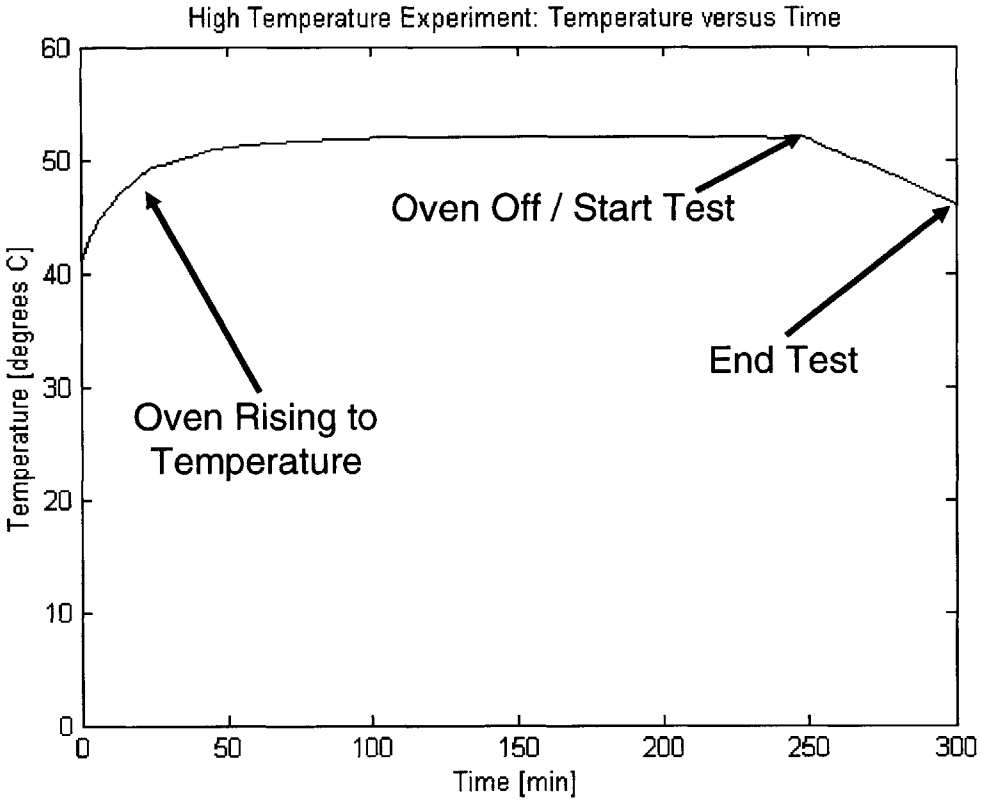

Figure 5.10: Oven Temperature Versus Time

5.4.1 Test Setup

The test setup for this experiment is the same as the general setup presented in Fig. 5.1. The DUT was situated in the oven (as it was for the last two experiments) and its electrical connections left intact. The device was thoroughly discharged before the experiment by short-circuiting the terminals with the copper shorting bars.

The experiment would be conducted with the device in the oven and by using dry ice as the coolant. The oven would serve as an insulated enclosure for the experiment. Figure 5.15 shows the DUT and dry ice in the enclosure. An additional tray was placed in the oven above the DUT. The tray was used to hold a quantity of dry ice. The dry ice did not touch the device or the thermocouple.

With the dry ice placed in the oven, the door was closed and the temperature measurements began. Figure 5.16 gives a plot of temperature versus time. The thermocouple used to measure the temperature was placed on the top of the device, in contact with the alu-

	NessCap 2500 F DLC		
	Resistance (Ω)	*Capacitance* (Farad)	*Time Constant* (second)
Fast	0.000421	2651	1.12
Medium	0.04601	322.3	14.8
Slow	0.6333	719.5	456

Table 5.2: Extracted Parameters for the 2500 F NessCap DLC Model (High Temperature)

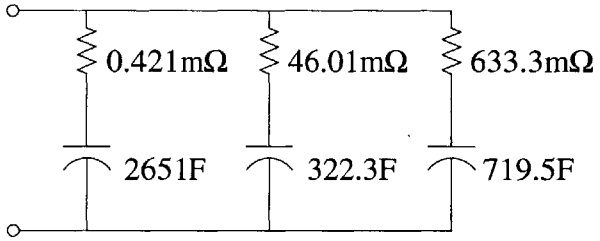

Figure 5.11: Extracted High Temperature Model for 2500 F NessCap DLC

minum casing. It can be seen from the plot that the temperature decreased rapidly once the dry ice was introduced to the system. The target temperature was $\sim -30\,^{\circ}\mathrm{C}$. While the device was being cooled down, it was determined that with the quantity of dry ice in the enclosure, the temperature, as measured by the thermocouple, would decrease below the target temperature. After ~135 minutes the temperature on the device's casing was measured at $\sim -39\,^{\circ}\mathrm{C}$, dry ice was removed from the enclosure (as can be seen in Fig. 5.16) and the temperature changes continually observed. The temperature rapidly increased to $\sim -35\,^{\circ}\mathrm{C}$ and then rose slowly and steadily. After an additional 200 minutes, the temperature measured by the thermocouple rose to $\sim -27\,^{\circ}\mathrm{C}$, and the experiment began. At the conclusion of the 50 minute experiment, the temperature was measured at $\sim -25\,^{\circ}\mathrm{C}$.

5.4.2 Results

The experimental "modeling" profile was run for this test as it was for the previous two. The device after being held at in a low temperature environment for an extended period of time received a pulse of constant current until the terminal voltage of the device reached ~0.5 V. Current and voltage measurements were taken during the experiment and collected at its conclusion. The gathered data was then examined using the modeling procedure of Chapter 3. Figure 5.17 shows the derived circuit model for this experiment. Table 5.3 summarizes the model's parameters and time constants.

The model was then used with the Simulink™/Matlab® program previously mentioned

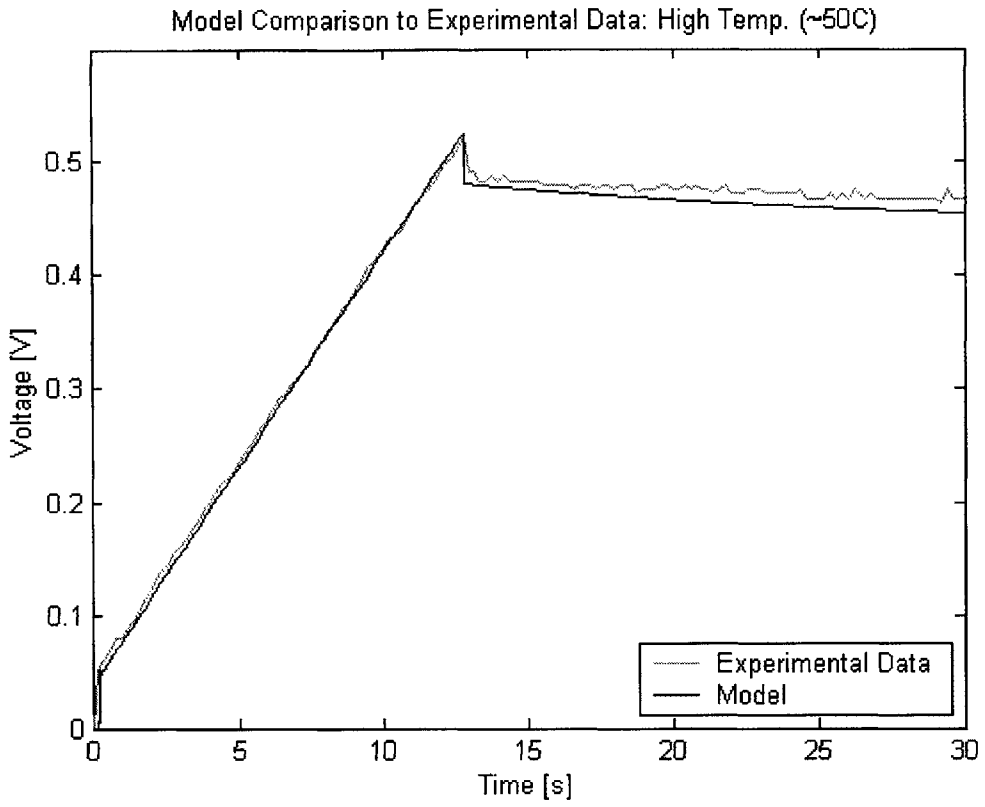

Figure 5.12: High Temperature Model Comparison for 2500 F NessCap DLC (0 to 30 s)

and Figs. 5.18 - 5.20 generated. Figure 5.18 shows the first 30 s of the experiment and gives a comparison of the model's performance. From this illustration, it can be seen that the model performs very well as compared to the device.

Extended time scales (0 to 300 s and 0 to 3000 s) are shown in Figs. 5.19 & 5.20 respectively. It can be seen from Fig. 5.19 that the model fits the 0 to 300 s data very well and also provides a good fit for the data shown in Fig. 5.20.

5.5 Conclusion

The three experiments presented in this chapter were performed so that the temperature trends that are characteristic of DLCs could be investigated. The investigation of such trends is a necessary step in implementing this technology in automobile (or other applications that are subjected to hot/cold environments).

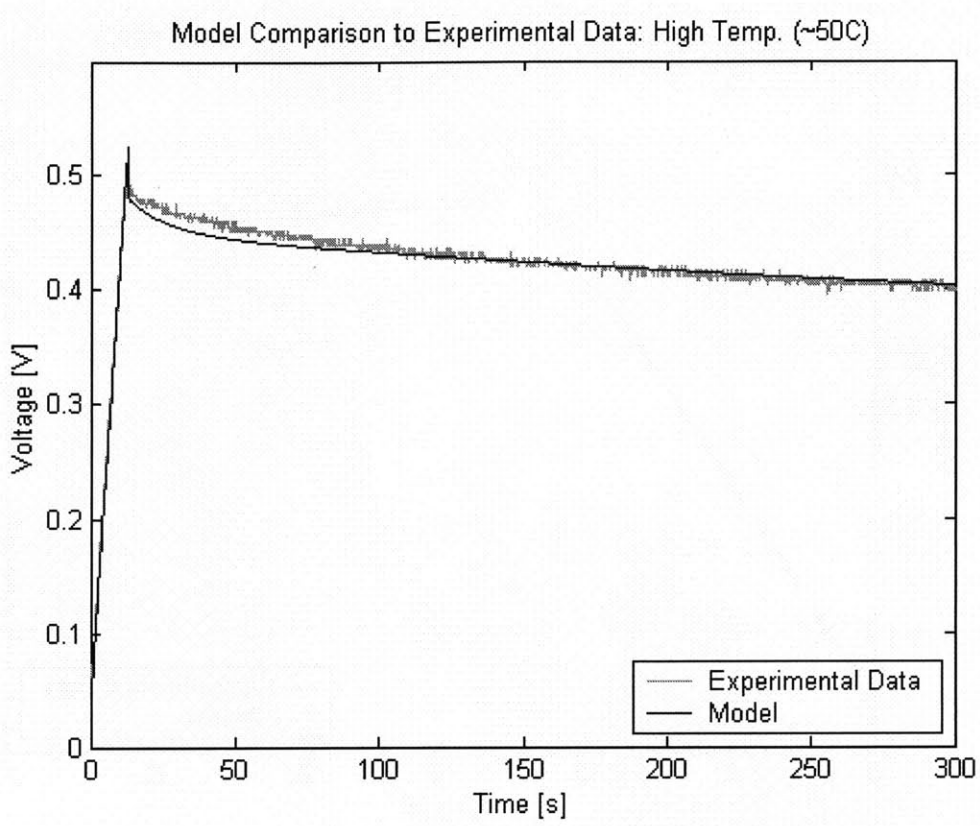

Figure 5.13: High Temperature Model Comparison for 2500 F NessCap DLC (0 to 300 s)

Table 5.4 summaries information pertaining to the three experiments. As can be seen in Table 5.4, for each experiment, the DUT received a pulse of current approximately 12.6 s in duration. Additionally, the terminal voltage of the initially discharged DLC reached approximately 0.52 V at the conclusion of the current pulse.

The next table, Table 5.5, summaries the resistance values calculated for the three model (room temperature, high temperature, and low temperature models). As can be seen from this summary, the resistance of the fast branch (i.e., R_f) does not appear to be effected considerably by the changes in temperature used in these experiments. This is an important piece of information as it suggest that the R_f value can be considered relatively constant (about 0.4 - 0.5mΩ) over a wide window of operating temperatures.

The resistance values for the medium branch do show some change over temperature. Using the room temperature as a starting point for the comparison, the R_m value can be seen to increase at the lower temperatures. An increase of resistance is to be expected at lower temperatures as at a low enough temperature, the electrolyte of the device will freeze. The

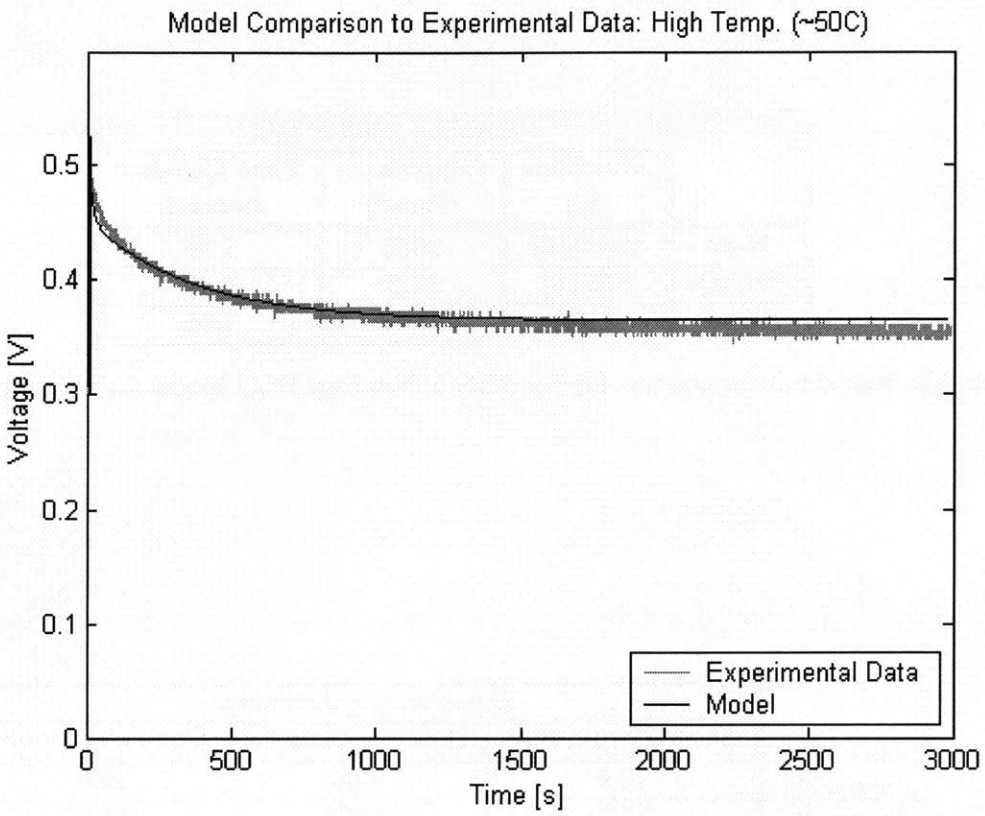

Figure 5.14: High Temperature Model Comparison for 2500 F NessCap DLC (0 to 3000 s)

manufacture's low range of operating/storage for this device is $-40\,^{\circ}\mathrm{C}$ while the experiment was performed at $\sim -25\,^{\circ}\mathrm{C}$. As for the medium resistance value for the high temperature experiment, the calculated value shows little, if any, change. The difference in temperature between the room temperature experiment and the high temperature experiment is very little (relative to the difference between the low temperature and room temperature experiments) which does not allow the difference in R_m to be noticed with the precision of this experimental setup and derivation procedure. Not much information has been determined from this parameters change at the higher temperature, although, it should be noted that the "high" temperature ($\sim 50\,^{\circ}\mathrm{C} \cong \sim 122\,^{\circ}\mathrm{F}$) is, in fact, not very high.

The slow resistances of the three experiments do show more deviation from on another. Again, using the room temperature calculated value of R_s as a starting point, the slow resistance value found from the low temperature experiment shows an noticeable increase ($\sim \times 2$). And the R_s value found from the high temperature data shows a noticeable decrease.

Table 5.6 gives a summary/comparison of the calculated capacitances of the three models.

	NessCap 2500 F DLC		
	Resistance (Ω)	*Capacitance* (Farad)	*Time Constant* (second)
Fast	0.000413	2575	1.06
Medium	0.07101	91.3	6.49
Slow	2.088	279.7	584

Table 5.3: Extracted Parameters for the 2500 F NessCap DLC Model (Low Temperature)

	Experimental Summary		
	Room Temperature	*High Temperature*	*Low Temperature*
$t_{charge}(s)$	12.6	12.6	12.6
$V_{t,max}(V)$	0.520	0.524	0.528

Table 5.4: Experimental Comparison

	NessCap 2500 F DLC		
	Fast Resistance (R_f)	*Medium Resistance* (R_m)	*Slow Resistance* (R_s)
Room Temperature	0.000508	0.04562	0.988
High Temperature	0.000421	0.04601	0.633
Low Temperature	0.000413	0.07107	2.088

Table 5.5: Extracted Resistance Parameters for the 2500 F NessCap DLC Model

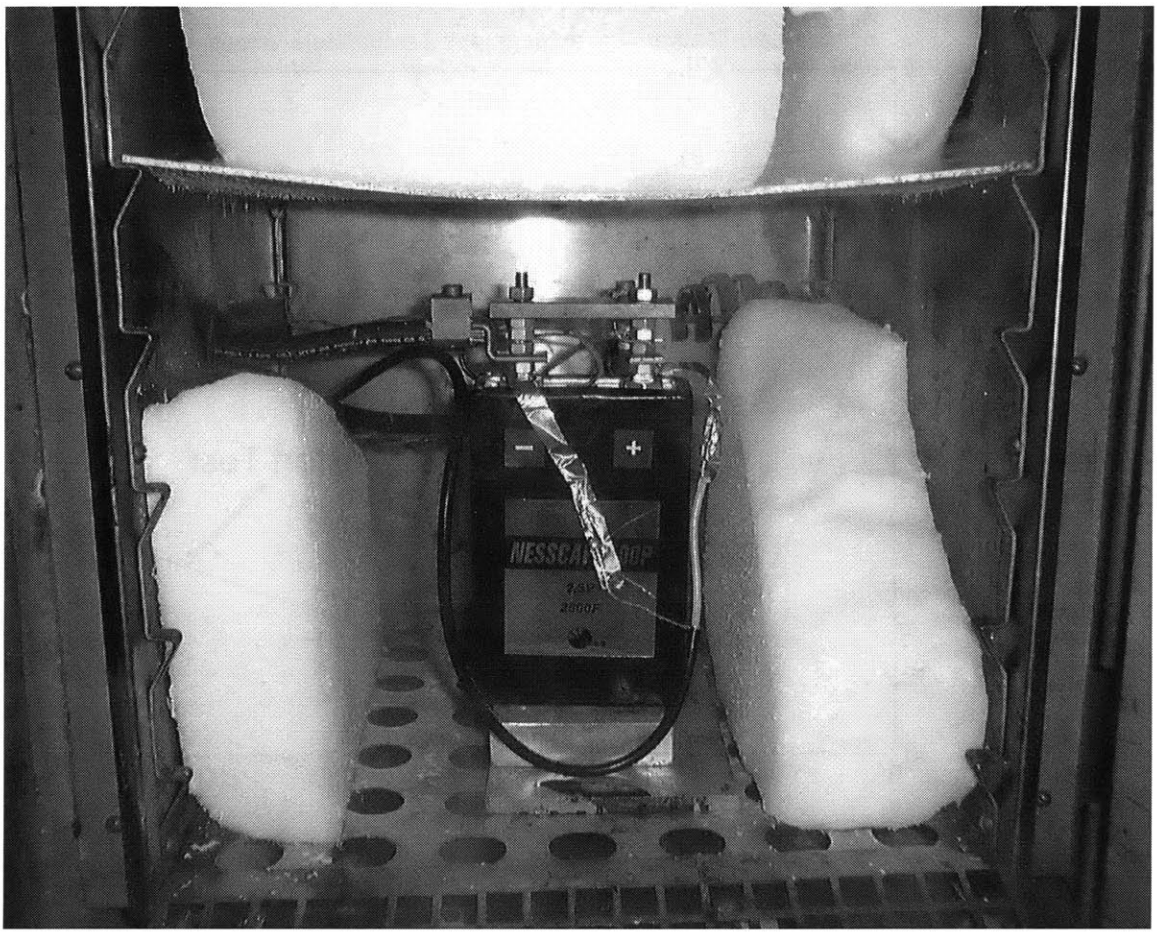

Figure 5.15: DLC in Oven with Dry Ice

Looking first at the fast branch capacitance (C_f), the capacitance value is not seen to change significantly if any (within the accuracy of the measurement equipment used). This comparison would suggest, as its counterpart did for the R_f values, that the C_f value may not show much deviation over a wide range of temperatures.

The comparison of the C_m values shows that a significant decease in capacitance is seen for the low temperature experiment, an expected phenomenon assuming that the electrolyte is losing viscosity as the temperature decreases closer to it's freezing point and ionic migration is decreased (thus slowing/preventing the ions from moving to the solid/liquid interface and forming a capacitance which results in a decrease in effective surface area of the electrode material). On the other hand, the C_m value calculated for the high temperature experiment shows an increase in capacitance.

The slow capacitance values for the three experiments again show some deviation from one

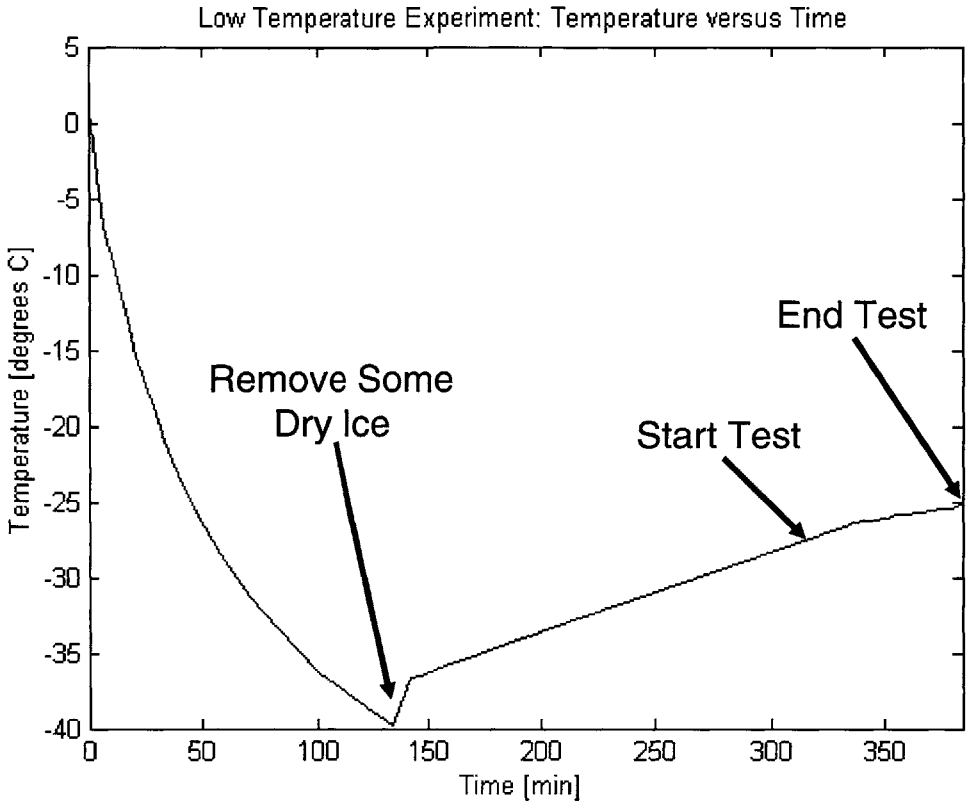

Figure 5.16: Temperature Versus Time

another. The C_s for the low temperature experiment shows a decrease in capacitance (as the C_m value did) and the value of C_s for the high temperature experiment showed an increase as compared to the room temperature value.

The time constants of the individual branches are summaries for each of the three experiments in Table 5.7. It is interesting to note that the time constants for the room temperature test and the high temperature test are very similar for their respective branches. The medium and slow time constants for the low temperature experiment show some deviation from the base-line experiment.

Figures 5.21 - 5.23 give a comparison of the device's performance for the three experiments. As shown in Table 5.4, the charging pulse of current was approximately the same duration for each of the experiments. And as mentioned previously, the setup configuration received little change for the three experiments (i.e., the current source was dialed in at 100.0 A and not changed during the course of these experiments). Additionally, Table 5.4 showed that the device reached approximately 0.52 V for each of the experiments.

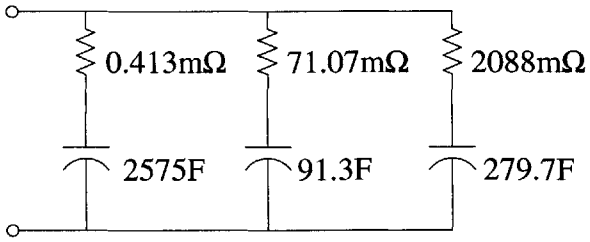

Figure 5.17: Extracted Low Temperature Model for 2500 F NessCap DLC

	NessCap 2500 F DLC		
	Fast Capacitance (C_f)	*Medium Capacitance* (C_m)	*Slow Capacitance* (C_s)
Room Temperature	2641	148.1	618.5
High Temperature	2651	322.3	719.5
Low Temperature	2575	91.3	279.7

Table 5.6: Extracted Capacitance Parameters for the 2500 F NessCap DLC Model

Figure 5.21 illustrates the three voltage curves for 0 to 30 s. As can be seen in this figure, the individual curves are indistinguishable during the charging phase (i.e, 0 to 12 s). From 12 s to 30 s the curves only show a little deviation from one another.

Looking on the time scale of 0 to 300 s (Fig. 5.22), the deviation between the three curves becomes very apparent. The low temperature curve is seen to show a slope that appear to be close to zero on this scale. Whereas, the high temperature curve shows that its voltage is decreasing at a greater rate than the other two curves.

The final plot, Fig. 5.23 illustrates the 0 to 3000 s time scale. In this plot, the three curves are performing very differently. The low temperature curve has maintained much more of it's initial voltage throughout the experiment. And the high temperature experiments curve has decreased the most of the three.

Looking at Figs. 5.21 - 5.23 and considering the model parameters presented in Tables

	NessCap 2500 F DLC		
	Fast Time Constant (τ_f)	*Medium Time Constant* (τ_m)	*Slow Time Constant* (τ_s)
Room Temperature	1.34	6.8	611
Low Temperature	1.12	14.8	456
High Temperature	1.06	6.5	584

Table 5.7: Extracted Time Constants for the 2500 F NessCap DLC Model

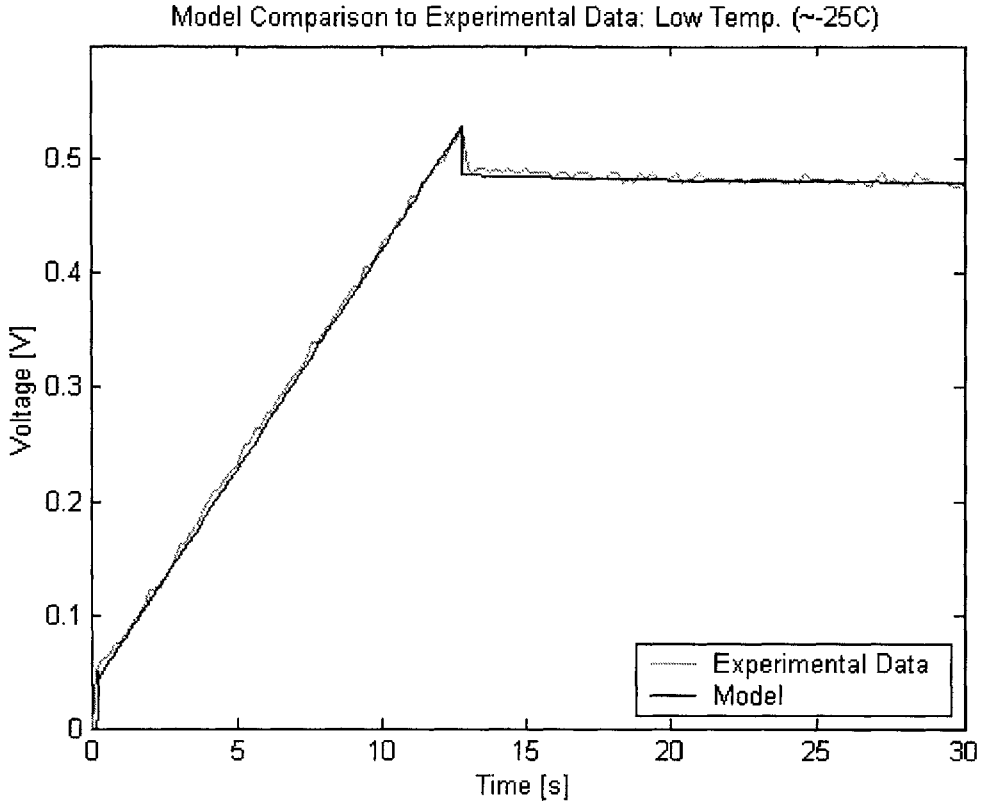

Figure 5.18: Low Temperature Model Comparison for 2500 F NessCap DLC (0 to 30 s)

5.5 & 5.6, one can begin to understand the phenomenon at work. In the case of the low temperature experiment, the voltage changed very little during the course of the experiment (relative to the other two plots). Considering that the electrolyte solution's viscosity decreased do to the temperature decrease (resulting in a higher resistance for the medium and slow branches), it is understandable that the ionic migration would be decreased. This decrease in migration of ions, results in a reduction in the formation of capacitance (as compared to the room temperature experiment) since the ions of the electrolyte much move/line up at the solid/liquid interface. If the ions require a longer time due to the higher resistance, this would appear as a lower capacitance value in the derived mode (as we saw in Fig. 5.6). It should be noted that the surface area of the bulk electrode structure would still posses the same surface area measurements during these three experiments, but that the reduction in ion migration results in the pores of the electrode structure from being "as" populated and hence a lower capacitance in measured for a comparable time scale.

Using the information regarding the high temperature curve in Fig 5.23 and the capacitance values of Table 5.6, it appears that the ion migration has increased (relative to the room

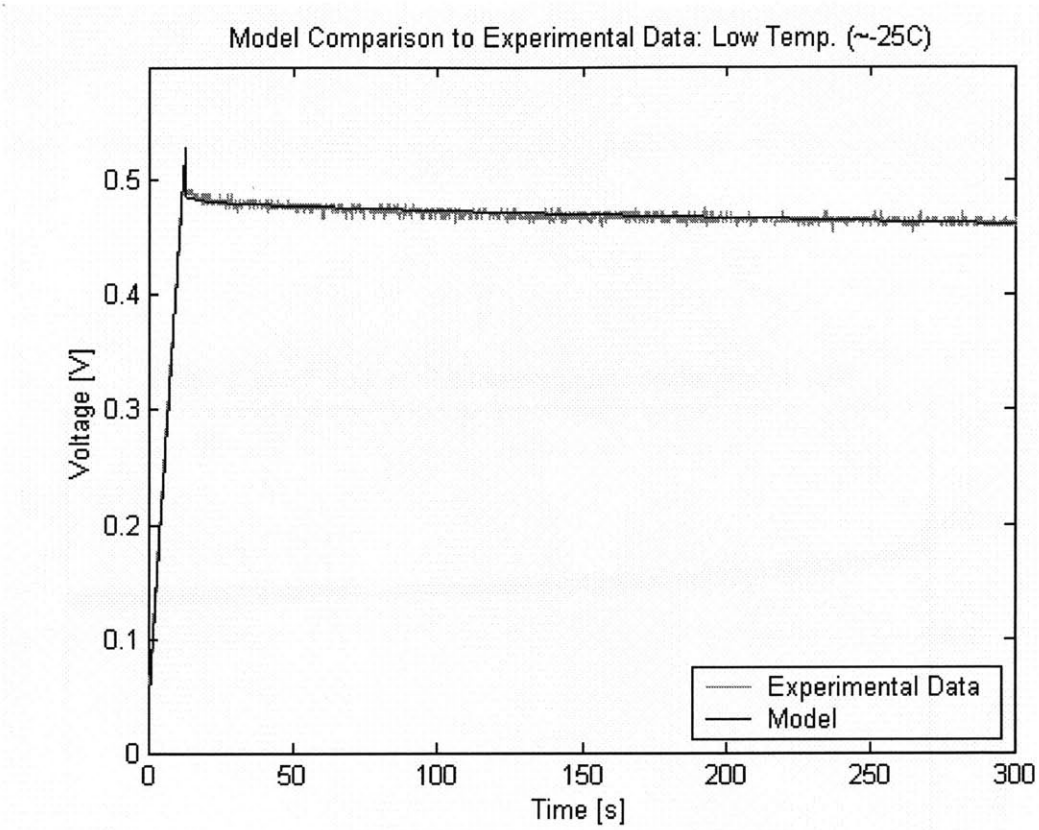

Figure 5.19: Low Temperature Model Comparison for 2500 F NessCap DLC (0 to 300 s)

temperature experiment) with temperature. An increase in ion migration would result in a quicker decrease of terminal voltage, the pores becoming populated at a higher rate, and a higher calculated capacitance for a comparable time scale. Several limiting factors may come into effect and include: ion migration limited to the physical size of the pore opening (pore mouth), sufficient ion concentration within the electrolyte, and saturation of the pores.

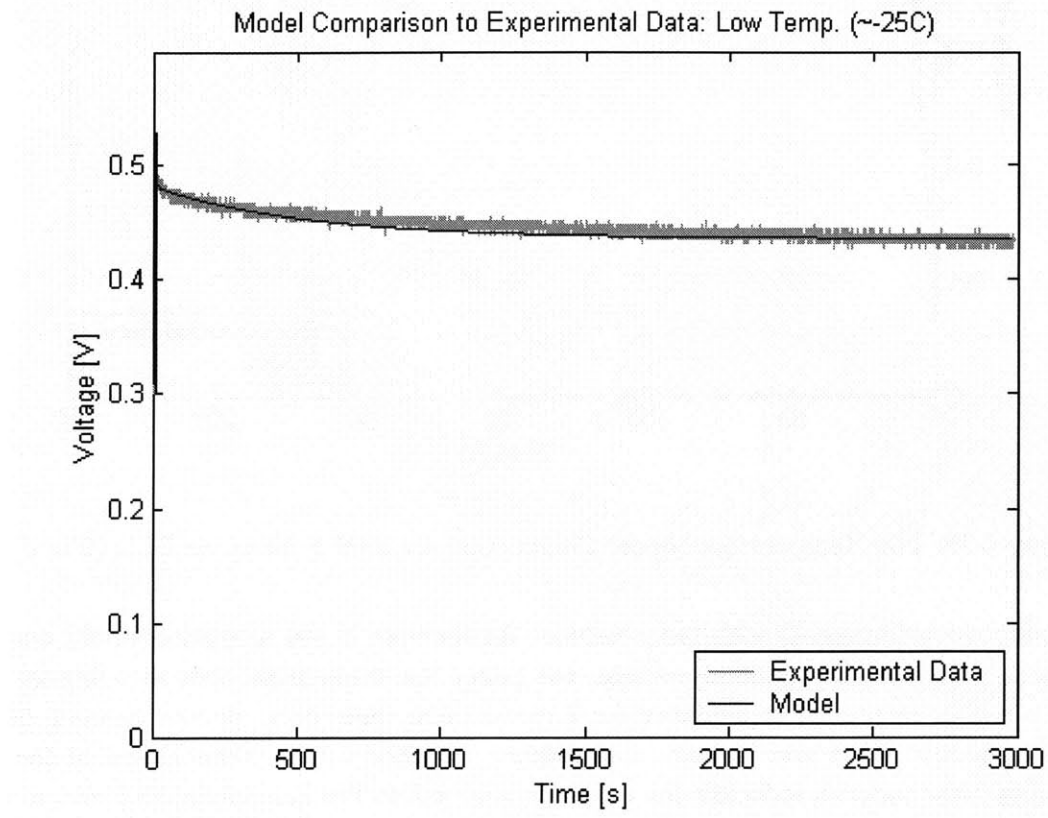

Figure 5.20: Low Temperature Model Comparison for 2500 F NessCap DLC (0 to 3000 s)

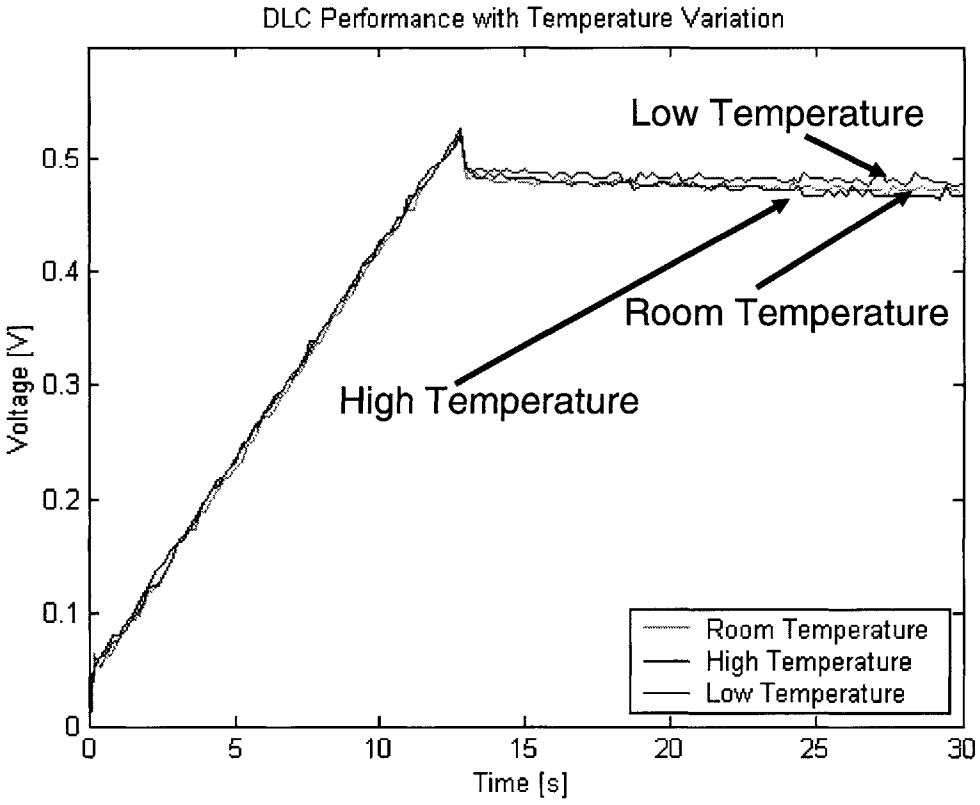

Figure 5.21: DLC Performance with Temperature Variation (0 to 30 s)

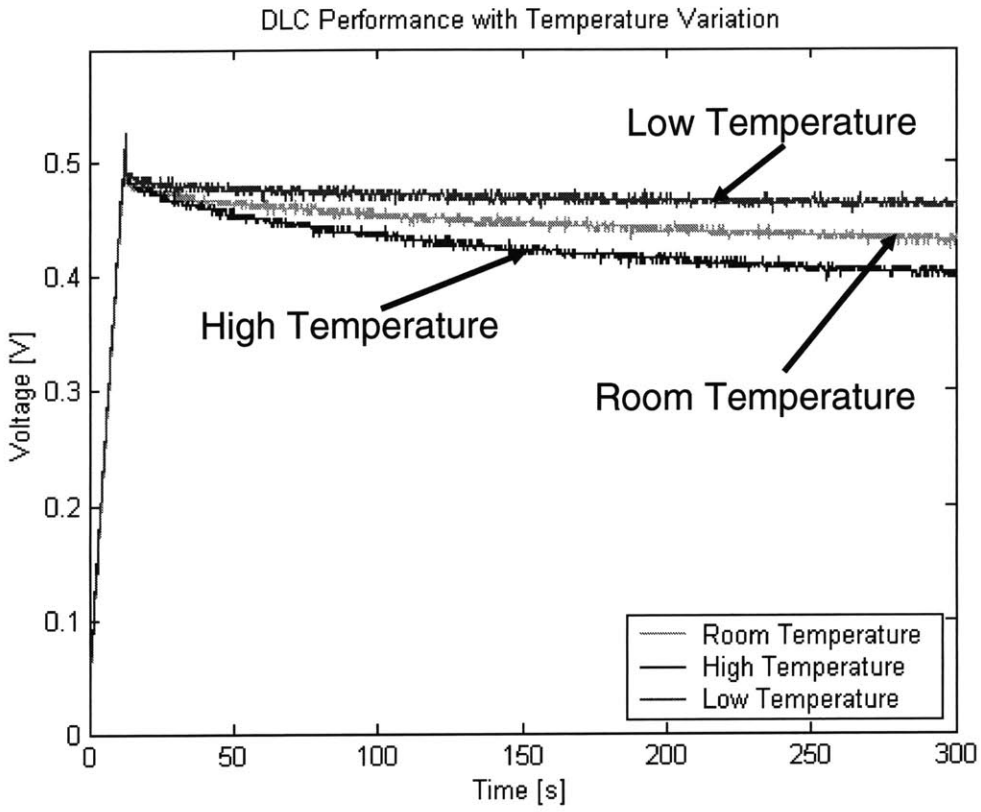

Figure 5.22: DLC Performance with Temperature Variation (0 to 300 s)

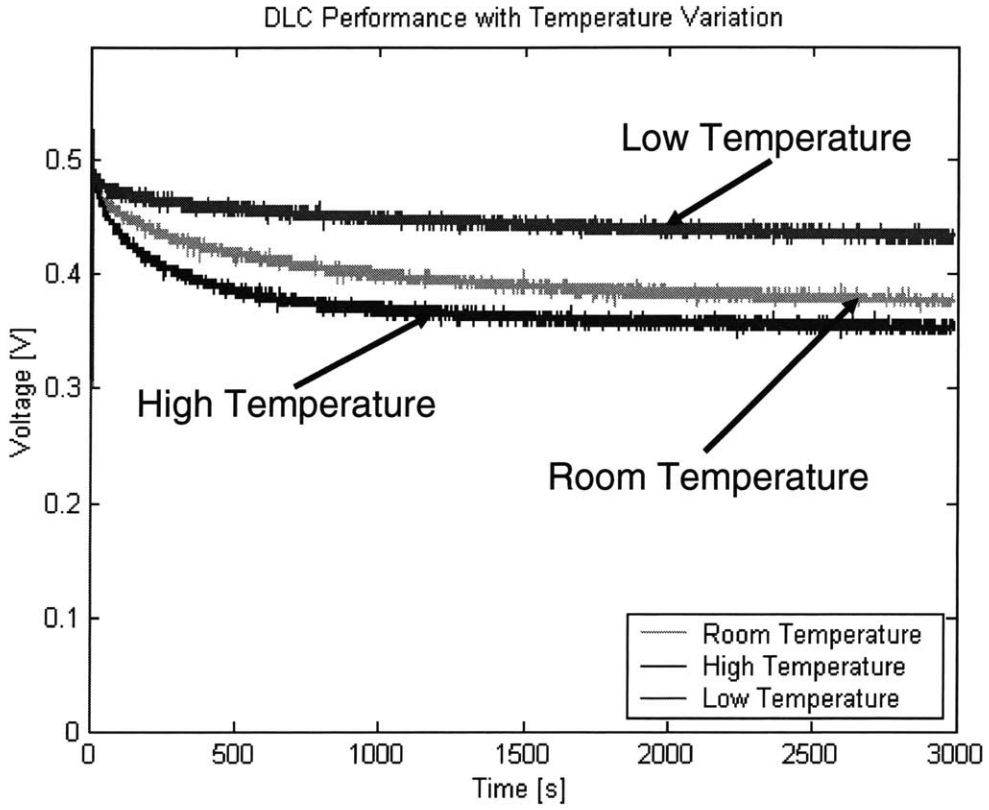

Figure 5.23: DLC Performance with Temperature Variation (0 to 3000 s)

Chapter 6

Modeling of the DLC's Nonlinear Capacitances

6.1 Introduction

A model extraction procedure for double layer capacitors was presented in Chapter 3. It was stated at that time that the device exhibits a nonlinear voltage dependent capacitance. As this is an inherent feature of these devices, the investigation and characterization of this phenomenon is required so that the performance of these devices in advanced electrical systems can be understood and predicted. This chapter presents the modeling of this phenomenon.

Furthermore, an important goal for this project was to produce a procedure of modeling the DLC's nonlinear behavior in such a way that could be highly accurate, but at the same time simple in terms of derivation (calculations, measurements, and simulation). Complicated and specialized software, as well as extensive data measurements and tables were to be avoided if possible. The following procedure realizes all of these goals. It relies on the use of common engineering software, does not require extensive data tables, and provides a reasonably accurate fit to the experimental performance of the device.

It was mentioned in section 3.2 that in order to investigate the nonlinearities of the Nesscap 2500 F devices, some change in the test setup need occur. The test setup's current source was used to charge the device at a constant current of ~100 A (the source has a maximum rating of 120 A). Also mentioned in section 3.2, is the need to charge the device (from 0 to V_{max}) in a time interval that would minimize the charging of the medium and slow branches so that certain assumptions could be used during the model extraction procedure. Equation 6.1 shows that the change in voltage (ΔV) of the device is related to the change in charge ($\Delta Q = I\Delta t$) of the device and the device's capacitance. In order to charge this device to a higher voltage (e.g., 2 V) in the same time period, the current used to charge the device would have to be increased.

$$C = \frac{\Delta Q}{\Delta V} = \frac{I\Delta t}{\Delta V} \tag{6.1}$$

Alternatively, a device with a lower capacitance rating could be used with this test setup. In order to achieve a maximum voltage of 2 - 2.5 V with approximately the same charging current and interval, the new device would need to have approximately 1/5 the capacitance (~500 F) of the previous device (as the maximum voltage is increasing by ~×5). This rough calculation assumes a constant capacitance (e.g., the capacitance does not change with voltage).

Several manufactures of DLCs were investigated in the search of a carbon based DLC with a capacitance of ~500 F, an organic electrolyte (so as to have a high operating voltage), and one that was of a high current design. The Maxwell 450 F device was found and selected for experiment. Figure 6.1 illustrates this device.

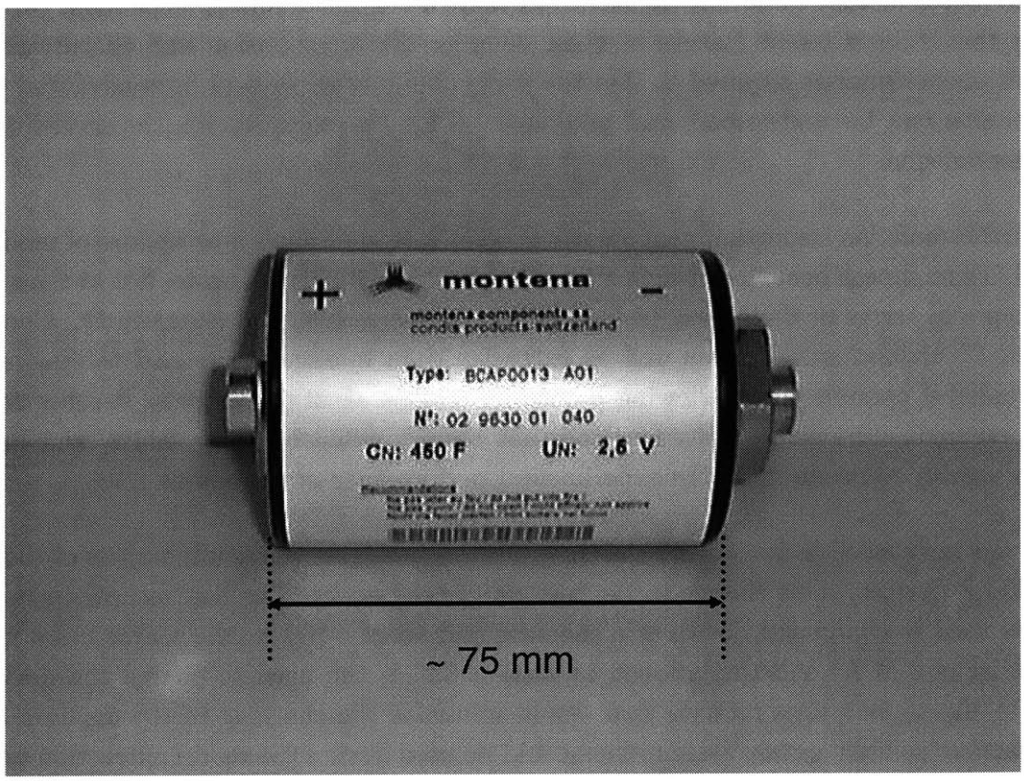

Figure 6.1: Maxwell 450 F DLC

The nonlinear capacitance of the DLC can easily be seen when fully charging an initially discharged device. Figure 6.2 shows the basic circuit for investigating the response of a DLC to a constant current source. The DLC (shown as the capacitor in the box) is charged with

a constant current for a period of time and then open circuited. The measurement of the device's voltage as a function of time (v(t)) is taken at the device's terminals. Figure 6.3 shows the response of the device to such an excitation. The device was initially discharged before being charged to ~2.25 V; the non-zero voltage at t=0^+ is a result of the voltage drop across the devices ESR once the current source is applied. A linear dashed line has been drawn from the starting point of the v(t) curve (at t = 0^+) to the point at which the current source was removed from the device (at t $\cong$ 11 s). Had the v(t) curve exhibited a constant slope (following the dashed line) during the charging of the device, this would have indicated that the device possesses a linear capacitance. Instead, the v(t) curve initially has a greater slope than the later portion of the curve. This "falling-over" of the curve indicates a changing capacitance (the capacitance the device exhibits is greater during the later part of the v(t) curve).

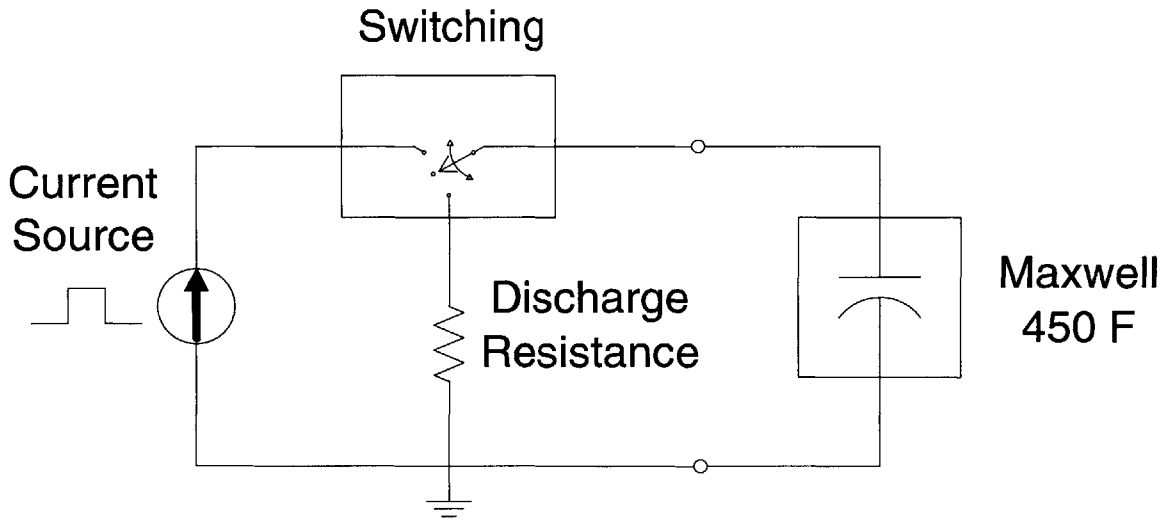

Figure 6.2: Basic Test Circuit

The model used when modeling DLCs (for short time periods) was presented in Fig. 3.2. In this model the capacitors are all constant (i.e., the do not change with voltage). Clearly, from Fig. 6.3, the DLC's capacitance changes at these higher voltages. The DLC model presented in Fig. 6.4 is similar to the model presented in Fig. 3.2, except that the "fast" capacitor is nonlinear with voltage. This nonlinear capacitor will be used to model the nonlinearity of the v(t) seen during charging.

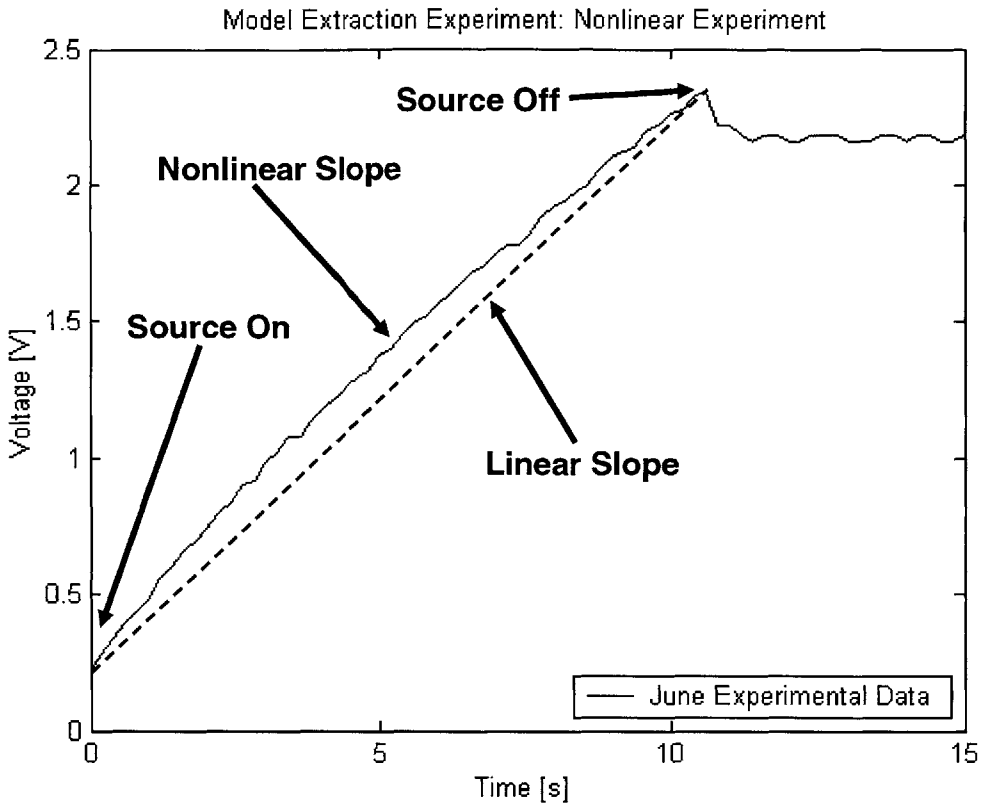

Figure 6.3: Charging of DLC

6.2 Test Setup

A diagram of the test circuit for this experiment is shown in Fig. 6.5. For the nonlinear model extraction procedure, the DUT (a Maxwell 450 F DLC) was charged with a constant current of ~100 A from a HP 6011A power supply set to run in constant current mode. The device was charged to approximately 2.25 V and then open circuited for the remainder of the 3000 s test. The current was measured with a A6303 current probe a AM 503B current amplifier. TDS 754D oscilloscope was used for the collection of the experimental data gathered by the current amplifier.

The terminal voltage of the DLC was measured as presented in Chapters 3 & 5. The terminal voltage of the device was measured by the oscilloscope via coaxial cable connected to copper foil at the terminals of the device. Copper foil was placed in the terminals of the device and stainless steel lugs were screwed into the terminals. Brass nuts were used to connect the copper ring terminals to the lugs. Figures 6.6 & 6.7 show illustrations of the connection at the device's terminals. This method of measuring the device's terminal

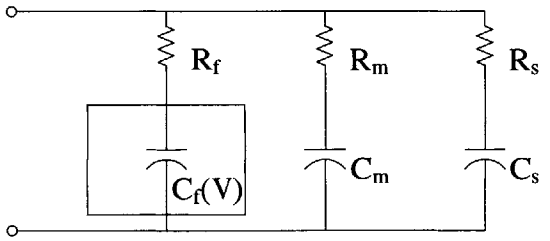

Figure 6.4: General Form of a Nonlinear "short-term" DLC Model

voltage is very important. The measurement of the terminal voltage on the copper foil gives the "true" terminal voltage of the device (outside of the package). An alternative method of measuring the device's voltage would be to connect the voltage probe to the copper ring connect. But this method of connection would not provide the "true" terminal voltage of the device. Rather the voltage measured would be the "true" terminal voltage minus the resistive drop between the device terminal and the steel lug, R_{CL}, minus the resistive drop between the steel lug and the copper terminal, R_{LT} (see Fig. 6.8). Even though the contact resistances between these components are quite small (on the order of mΩs) they are significant when trying to measure resistance parameters (i.e., R_f) of the model that are in the range of a fraction of a mΩ to a few mΩs.

Figure 6.9 show the laboratory setup of the test circuit. In this figure, the current amplifier, the current probe, the oscilloscope, the DUT, and the mechanical switch can be seen. Figure 6.10 shows a close up view of the laboratory setup. In this figure, the multimeter used to view the DUT's terminal voltage (during the experiment) can be seen. Also, the resistive load used to discharge the DUT (after the experiment) can be seen.

Figure 6.10 shows that the DUT for this experiment is part of a "cluster" of several (six) DLCs. The test setup constructed allows the testing of multiple (or a single) DLC(s). This experiment, the investigation and modeling of the nonlinear capacitance of DLCs, only requires the use of one DLC. Other experiments which use this same setup are interested in the performance of several DLCs at once.

Figure 6.11 illustrates in more detail the DLC "cluster." The cluster consists of six Maxwell 450 F devices all connected in series by copper buss bars. A copper "shorting" bar can be connected across devices 1 and 6 as shown in Fig. 6.10 to fully discharge the cluster. The six devices are all "standing" on their stainless steel lugs (as mentioned above) and mounted in a Plexiglas base. Copper foil is placed in the terminals of each device to provide a means of connection to the terminals for voltage measurements. The copper foil is connected to wires that run to the "interface board" where BNC connectors are mounted for connection to the oscilloscope. This board allows the voltage measurement of any of the six cells and

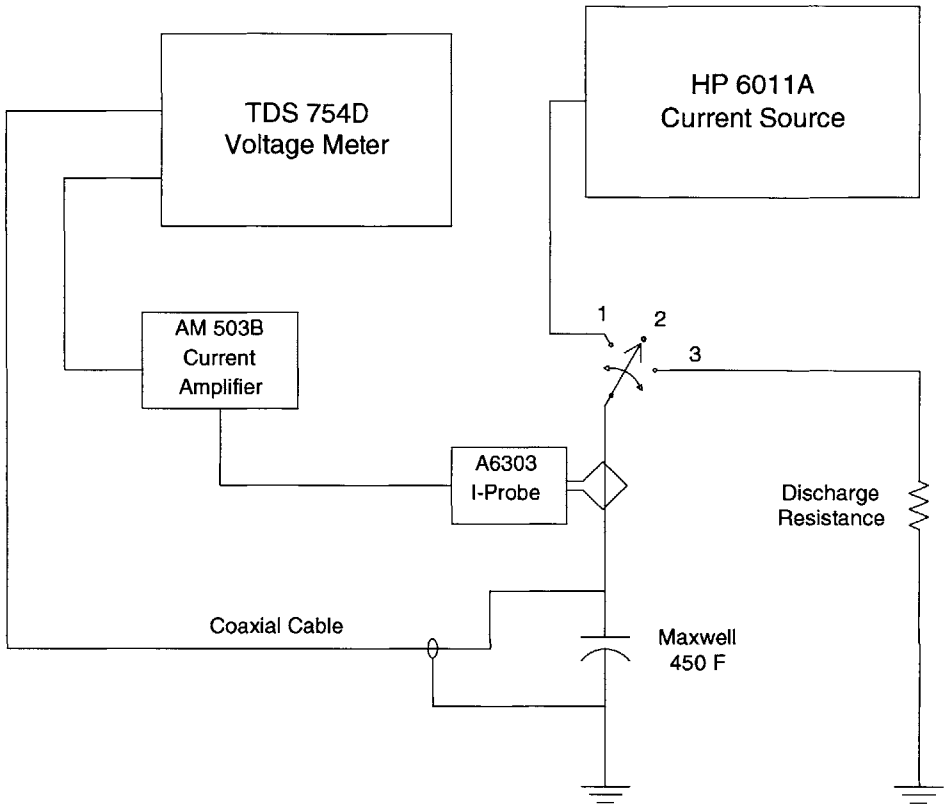

Figure 6.5: Basic Experimental Test Circuit

also allows the voltage measurement of the entire series chain.

As mentioned before, the measurement of the "true" terminal voltage is important for this experiment. The voltage measured at the BNC connector on the interface board is the "true" terminal voltage as it is at the terminals, even though there are contact resistances along the path from the device's terminal to the BNC connector. This assumption holds true as long as there is no current flowing along the path of the DLC's terminal to the oscilloscope. Given that the input resistance of the oscilloscope is extremely high (ideally infinite), it can be assumed that no current is flowing. This assumption does not hold true for the example presented in Fig. 6.8. The reason is that during the charging (or discharging) of the device, the current flowing into the device would cause a voltage drop across the contact resistance between the copper ring connector/stainless steel lug (R_{CL}) and a voltage drop across the contact resistance between the stainless steel lug/device's terminal (R_{LT}). With the device open-circuited (as it is during the open-circuit portion of the model extraction experiment), the voltage measured at the copper terminals would be the same as that measured at the terminals of the device.

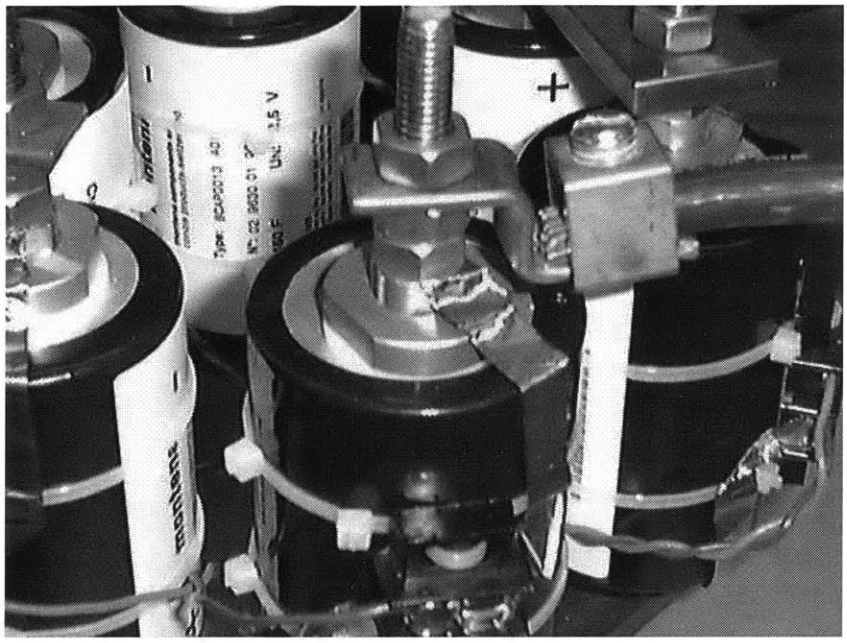

Figure 6.6: Copper Foil Connection to Device

6.3 Extraction Procedure

As mentioned previously, the capacitance of the device is nonlinear with voltage. Figure 6.12 shows that the slope of the $v(t)$ curve is initially different from its value at the end of the charging of the device; the capacitance is greater at the higher voltages than it is at the lower voltages. In order to model the voltage dependent capacitance, the capacitance of the model must be able to change (increase) with increasing voltage.

The modeling of this nonlinear capacitance uses a data table and the "Spline" function in Matlab®. The data table is a collection of capacitance calculations at different voltage levels of the device. That is, the capacitance is calculated at a low voltage level (e.g., during the first few seconds of charging) and then calculated at a high voltage level (e.g., due the last few seconds of charging). Additional data points can be determined in between the initial and final data points if needed. The Spline function will interpolate the values of the capacitances for the voltage levels between the data points given in the table.

The calculations for the other two capacitances (i.e., medium and slow capacitances) and the three resistance parameters are as presented in Chapter 3.

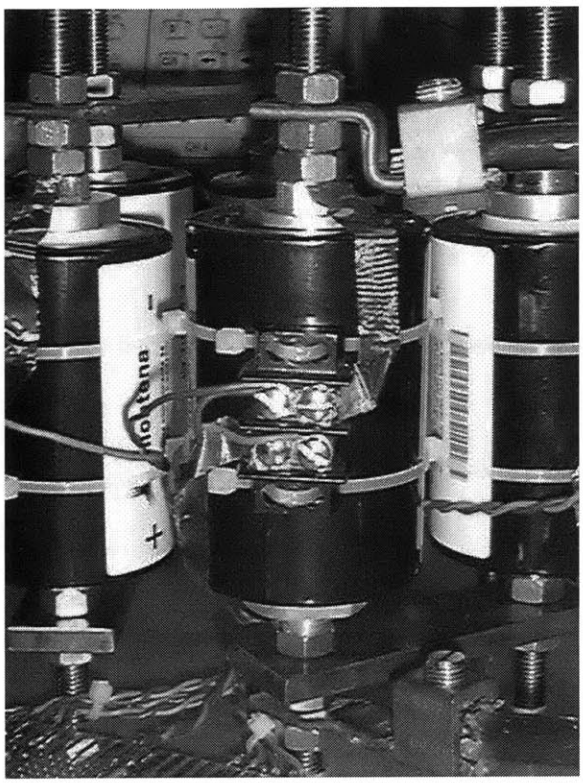

Figure 6.7: Connection of Device to Interface Board

6.4 Example of Extraction Procedure

The following is an example of the calculation of the nonlinear DLC model. This section shows the actual calculation of the nonlinear capacitance ($C_f(V)$) as needed when modeling the nonlinearities of the DLC and the calculations of the medium branch model parameters. The other parameters (R_f, R_s, and C_s) are presented at the end of this section. The calculation of the final three parameters is done exactly as presented in Chapter 3 (but substitute in the voltage dependent capacitance) and the calculations are not presented in an effort to avoid repetition. The assumptions made in Chapter 3 are still used in this modeling procedure.

6.4.1 Calculation of C_f

The DUT is initially discharged by short-circuiting the terminals of the device with a copper shorting bar (Fig. 6.10) for several days at room temperature. At t = 0, a pulse of constant current is applied to the device. Based on the relative resistances and time constants of the

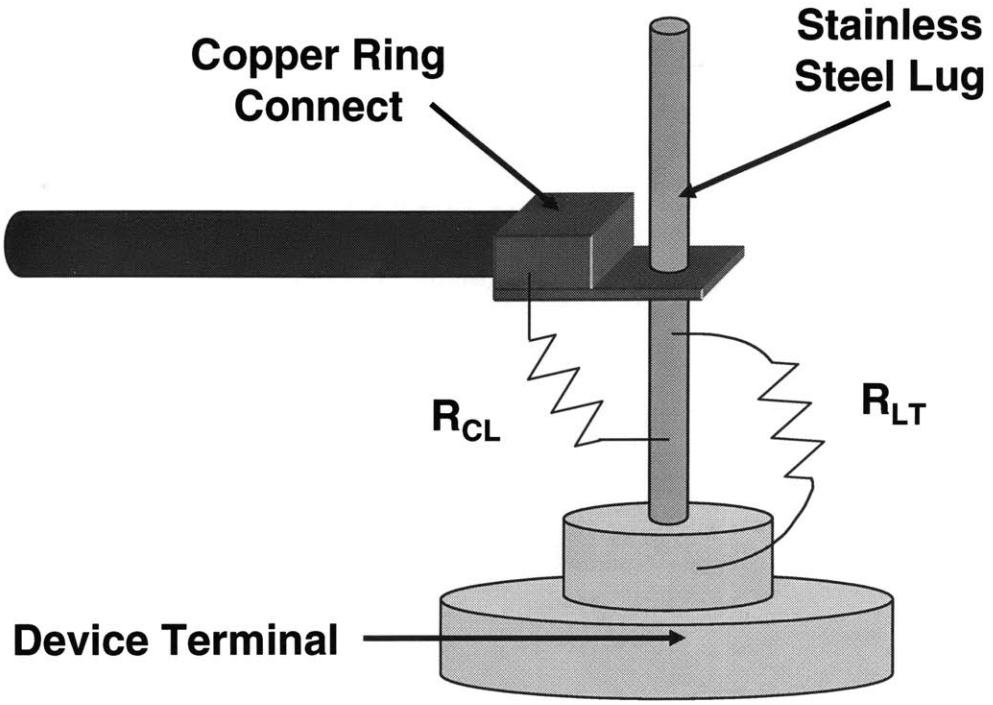

Figure 6.8: Illustration of Contact Resistances

branches, the charge stored in the device during this short period of time is assumed to be stored entirely in the fast branch.

The calculation of C_f begins with the assumption that the initial voltages of the three capacitors in Fig. 6.4 are 0 V and that the time constant of the fast branch ($\tau_f = R_f C_f$) is much less than the time constants of the medium and slow branches (see equation 6.2), and that the resistances of the three branches follows the relation stated in (6.3). Given that the charging interval is short (relative to the time constants of the medium and slow branches), the total charge delivered to the device is almost entirely stored in the fast branch capacitor.

$$\tau_f \ll \tau_m \ll \tau_s \tag{6.2}$$

$$R_f \ll R_m \ll R_s \tag{6.3}$$

In determining values for use in the "data table," it was chosen to start with calculating the initial and final capacitance values of the device to give a starting and an ending point for the Spline data. If more data was needed, more could be obtained to provide a better

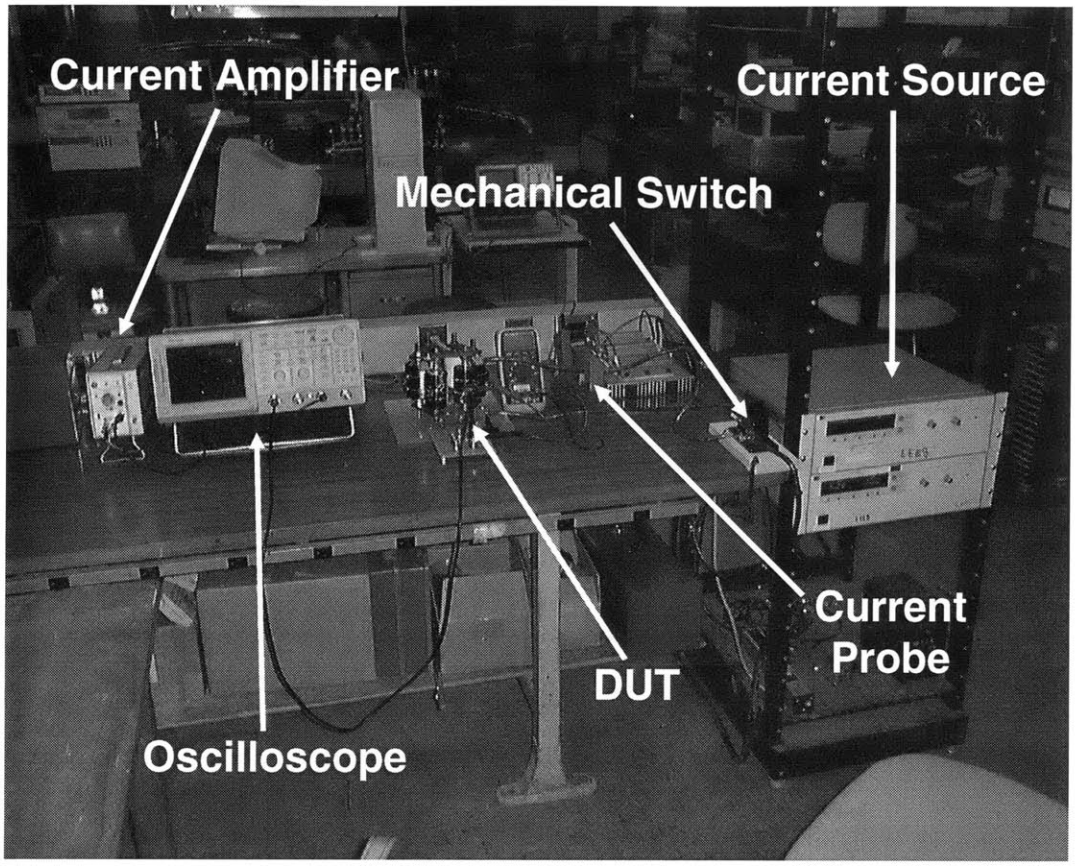

Figure 6.9: View of Test Circuit

fit to the experimental data. However, it will be shown that the change in capacitance with voltage appears to be approximately constant and that the initial and final values of C_f, with the use of Spline, is sufficient to model this trend. The interval used when determining data for the data table needs to be long enough so that the noise in the data will have a minimal effect on the calculation, but short enough that the change in voltage is nearly constant during that interval (i.e., the capacitance is nearly constant during that interval). The length of the interval chosen was 3 s. Figure 6.13 shows the two intervals used for the calculations. Figure 6.14 shows the charging current waveform and the two calculation intervals.

The initial capacitance ($C_{f,initial}$) was determined by looking at the first 3 s of the $v(t)$ curve. The value of $C_{f,initial}$ can be calculated by dividing the change in charge ($\Delta Q_{initial}$) by the initial change in voltage of the capacitor ($\Delta V_{C_{f,initial}} \cong \Delta V_{t,initial}$) over a given interval as shown in (6.4).

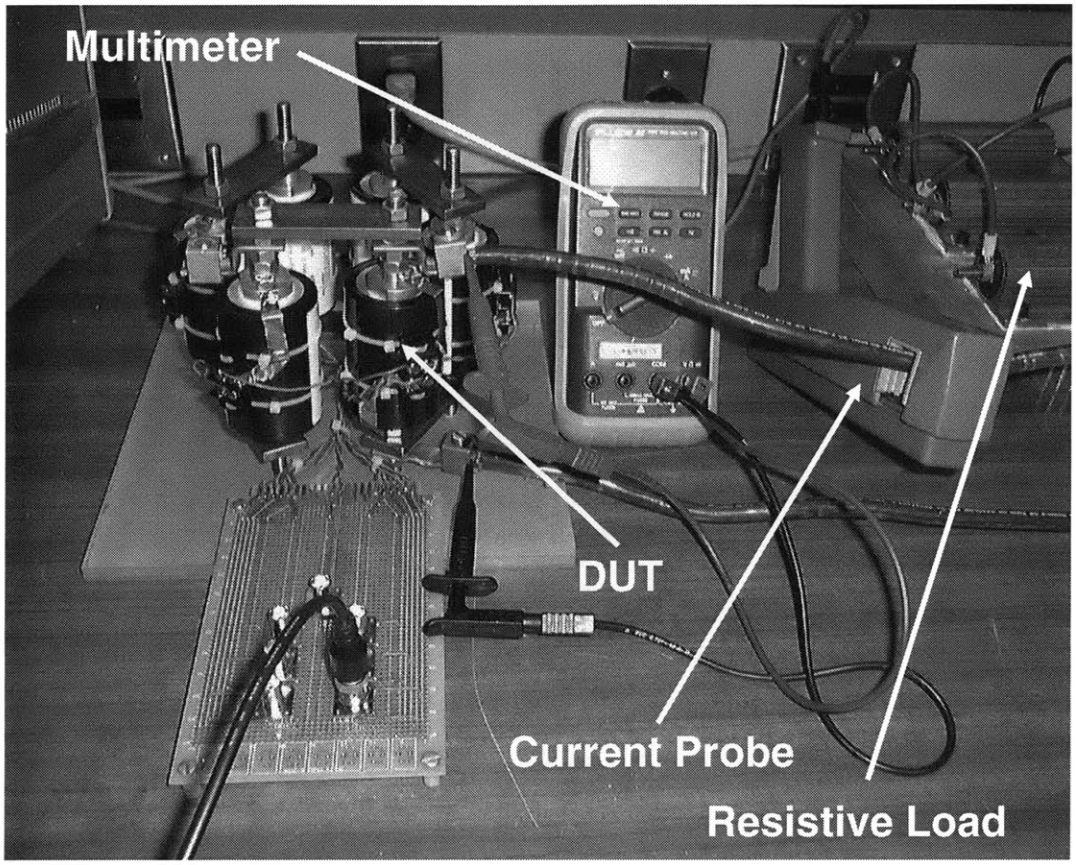

Figure 6.10: Close-up View of Test Circuit

$$C_{f,initial} = \frac{\Delta Q_{initial}}{\Delta V_{t,initial}} \tag{6.4}$$

The calculation of the delivered charge over the initial interval is found by measuring the current delivered to the DUT, the charging time, and by using (6.5) or alternatively stated, by taking the integral of the $i(t)$ waveform shown in Fig. 6.14 over the first 3 s. The measured value of $\Delta Q_{initial}$ was found to be 312.96 C and is shown as the shaded area (Q_1) under the curve in Fig. 6.15.

$$\Delta Q_{initial} = \int_0^{t=3s} i(t)dt \cong \Sigma(I \times \Delta t) \tag{6.5}$$

$$\Delta Q_1 = 312.96 \text{ C}$$

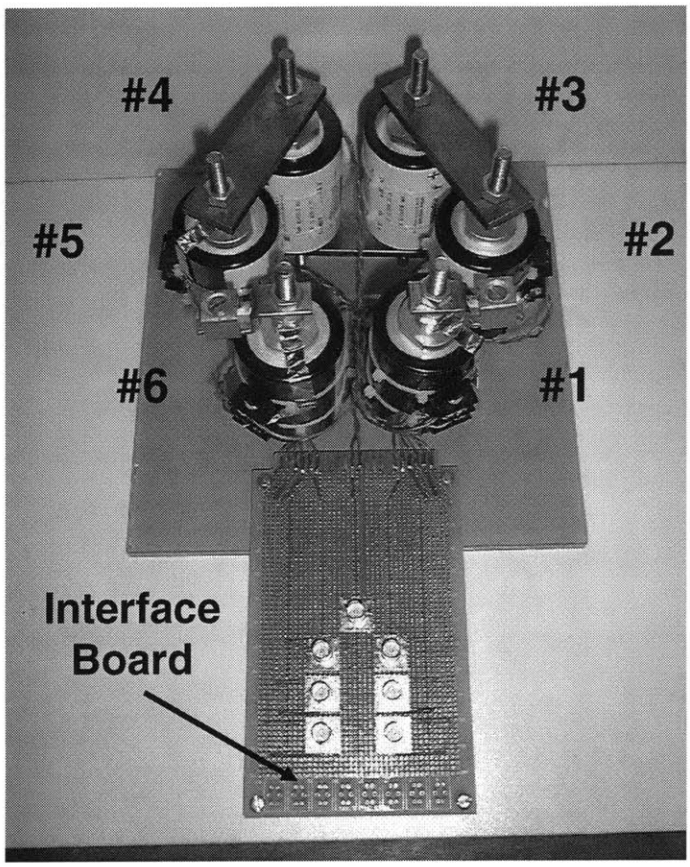

Figure 6.11: DLC "Cluster" and "Interface Board"

Using the change in voltage found in Fig. 6.16 during the initial 3 s of the charging interval ($\Delta V_{t,initial} = 0.76$ V) and (6.4), the calculated value of $C_{f,initial}$ is 411.8 F.

$$C_{\text{f,inititial}} = \frac{\Delta Q_1}{\Delta V_{\text{t,initial}}} = \frac{312.96 \text{ C}}{0.76 \text{ V}} = 411.8 \text{ F}$$

Since the capacitance (C_f) is a function of voltage, simply having the "initial" capacitance is not enough for the Matlab® model (i.e., the data table used to model the nonlinear capacitance). The corresponding voltage for this capacitance is the voltage as it appears across C_f, and not the terminal voltage (V_t). Figure 6.16 shows that the terminal voltage of the device is approximately 1 V at the end of the "initial" interval. Furthermore, there is an initial jump (at $t = 0^+$) of approximately 0.2 V due to the drop across R_f. The corresponding voltage for this value of capacitance is approximated by subtracting the resistive drop from the terminal voltage. This found value is 0.8 V.

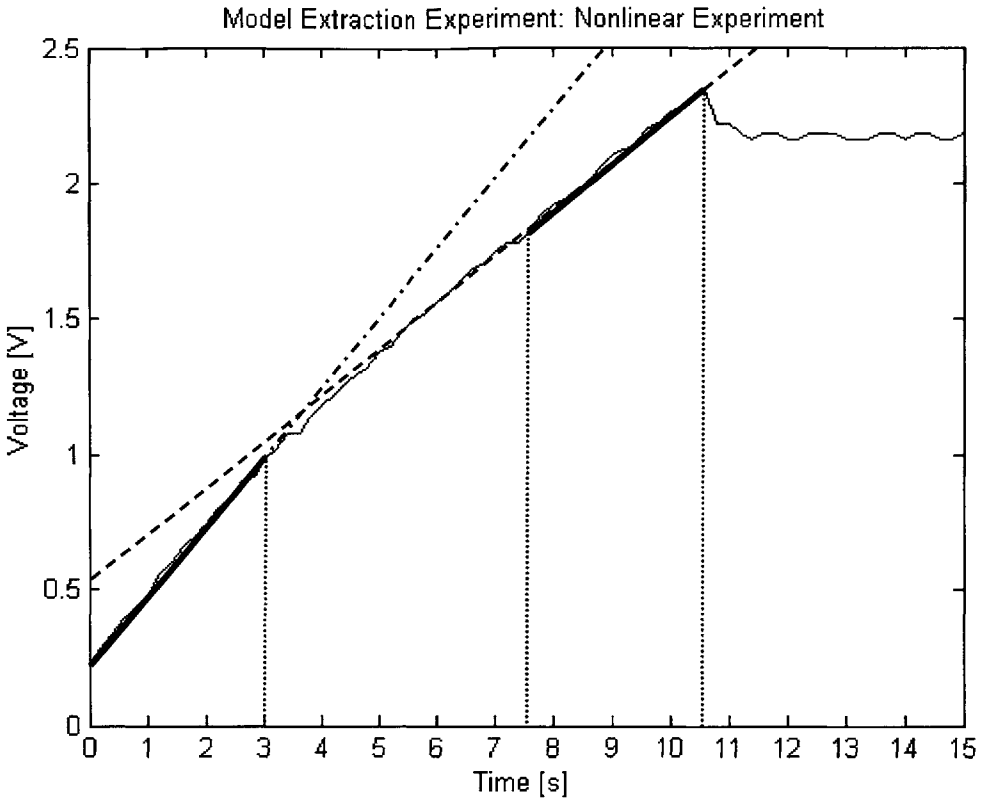

Figure 6.12: Initial and Final Slope of the Charging DLC

The final capacitance ($C_{f,final}$) was determined by looking at the last 3 s of the v(t) curve. The value of $C_{f,final}$ can be calculated by dividing the change in charge (ΔQ_{final}) by the final change in voltage of the capacitor ($\Delta V_{C_{f,final}} \cong \Delta V_{t,final}$) over a given interval as shown in (6.6).

$$C_{f,final} = \frac{\Delta Q_{final}}{\Delta V_{t,final}} \tag{6.6}$$

The calculation of the delivered charge over the final interval is found by measuring the current delivered to the DUT, the charging time, and by using (6.7) or alternatively stated, by taking the integral of the i(t) waveform shown in Fig. 6.14 over the last 3 s. The measured value of ΔQ_{final} was found to be 305.92 C and is shown as the shaded area (Q_2) under the curve in Fig. 6.15.

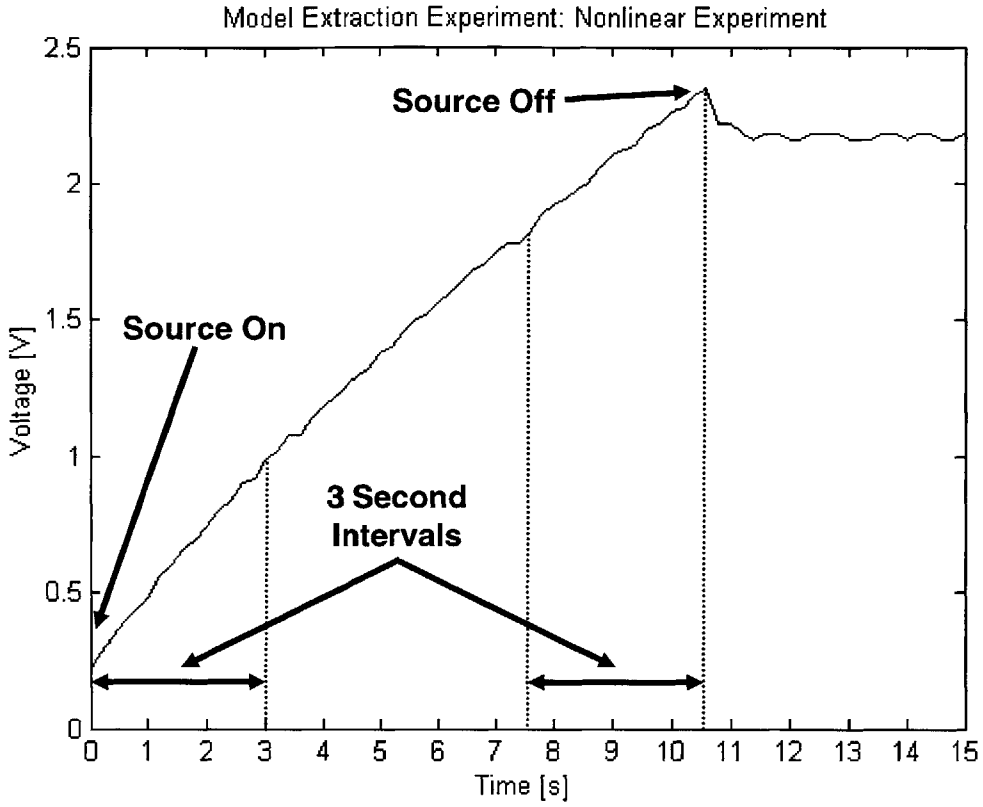

Figure 6.13: Initial and Final "Intervals"

$$\Delta Q_{final} = \int_{t=7.6s}^{t=10.6s} i(t)dt \cong \Sigma(I \times \Delta t) \tag{6.7}$$

$$\Delta Q_2 = 305.92 \text{ C}$$

Using the change in voltage found in Fig. 6.16 during the final 3 s of the charging interval ($\Delta V_{t,final} = 0.52$ V) and (6.6), the calculated value of $C_{f,final}$ is 588.3 F.

$$C_{\text{f,final}} = \frac{\Delta Q_2}{\Delta V_{\text{t,final}}} = \frac{305.92 \text{ C}}{0.52 \text{ V}} = 588.3 \text{ F}$$

Figure 6.16 shows that the terminal voltage of the device is approximately 2.3 V at the end of the "final" interval. The corresponding voltage for this value of capacitance is approximated by subtracting the 0.2 V resistive drop from the terminal voltage. The found value for this

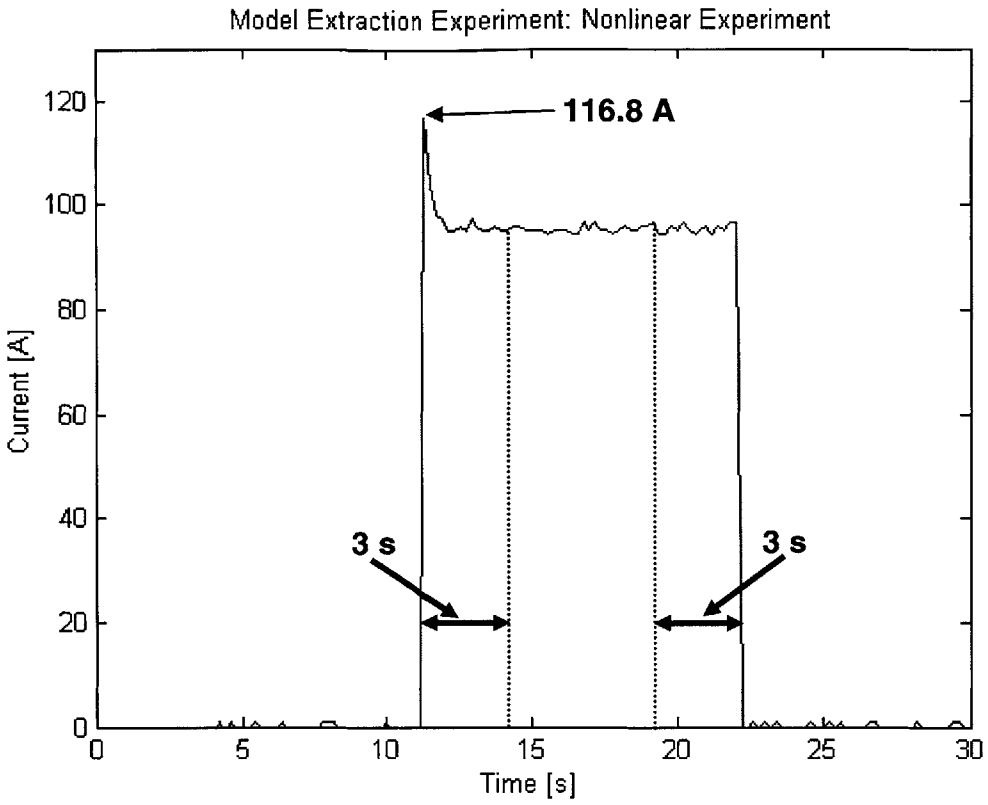

Figure 6.14: Pulse of Current use to Charge DLC

calculation is approximately 2.1 V. Table 6.1 gives the data table used for the Matlab® model.

It should be mentioned, that the initial "jump" in voltage (at $t = 0^+$) is found in this experiment to be approximately 0.2 V, but that the "drop" in voltage once the current source is removed from the device (at $t \cong 11$ s) is approximately 0.15 V. Shouldn't the two discontinuities in the voltage be equal? Actually, no. Remember, the assumption was made that the charging current is flowing entirely through the "fast" branch during the charging interval (so long as the interval is kept short). The longer the charging interval, the less the assumption can be relied on. At the beginning of the charging interval, the assumption is a very good one and the "jump" seen reflects the Thévenin resistance of the device (which is approximately R_f). If by the end of the charging, all the current is still flowing through the fast branch (and only in the fast branch), the two discontinuities would be the same (actually, if the medium branch began charging at the instant the charging pulse ended, the "drop" would be slightly greater as the drop across R_f would be reversed while C_f charged the medium branch). However, by the end of the charging interval, the current flowing

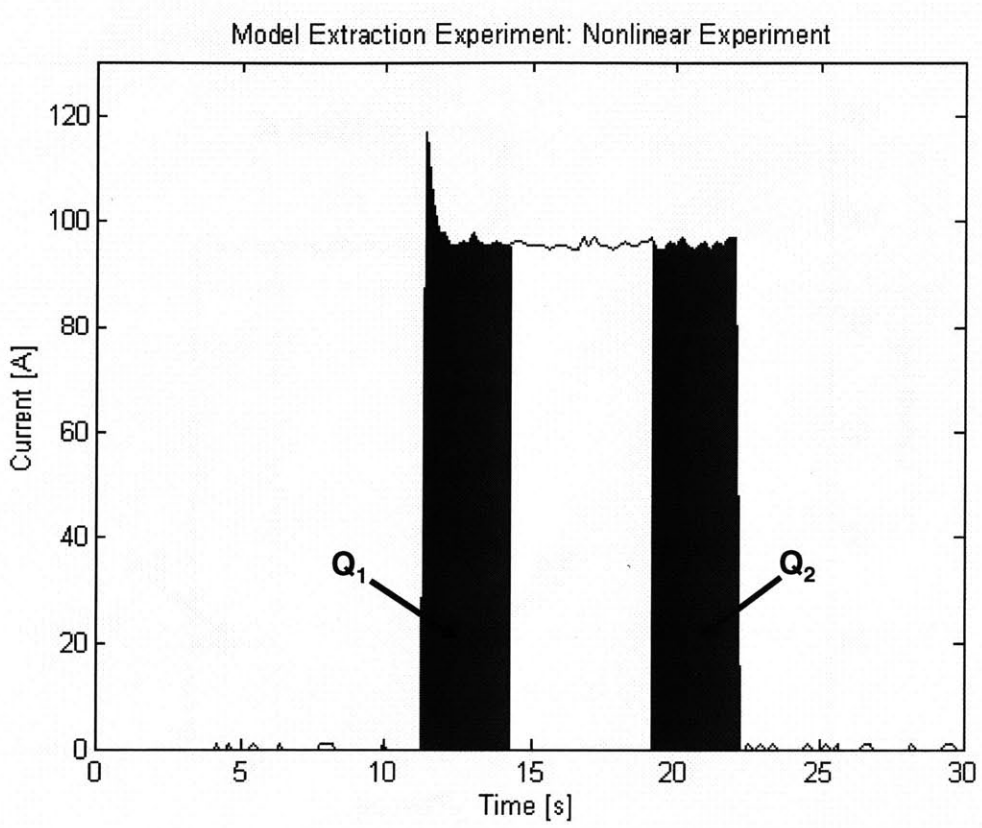

Figure 6.15: Charge (Q) Transferred to DLC

"beyond" the fast branch (say into the medium branch) has in reality, increased from the quantity initially (at t = 0^+). Therefore, the drop across R_f(t = 10.6 s) is less than the drop across R_f(t = 0^+). This is reflected in the discontinuity in voltage seen at the end of the charging interval. The quicker the device can be charged to its maximum voltage, the better the assumption holds that nearly all the charging current in stored in the fast branch.

Capacitance	*Voltage*
411.8 F	0.8 V
588.3 F	2.1 V

Table 6.1: Data Table for Matlab® Model

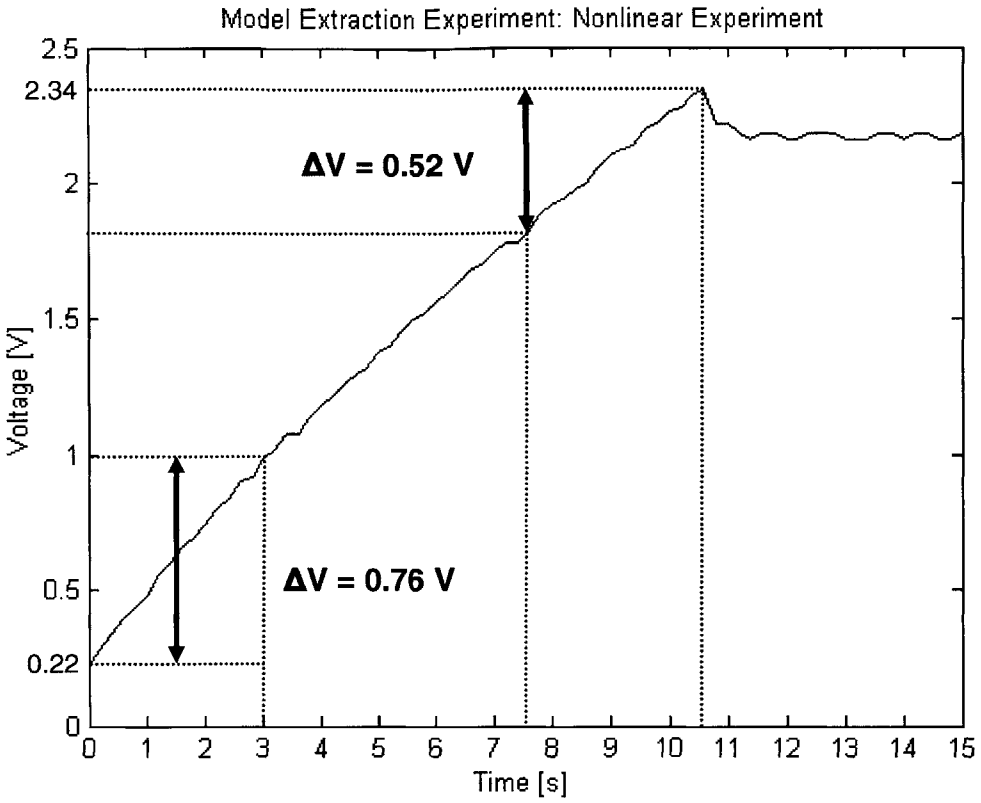

Figure 6.16: Change in DLC Terminal Voltage during Initial and Final Intervals

6.4.2 Calculation of R_m

The calculation of the resistance of the medium branch (R_m) follows the procedure outlined in Chapter 3 and is found immediately following the charging interval by using (6.8) and the assumption that the terminal voltage of the device corresponds to the voltage across R_m (i.e., $V_t = V_{R_m} + V_{C_m} = V_{R_m} + 0\text{ V} = V_{R_m}$). The capacitance value used in (6.8) needs to be approximated by looking at the voltage level of the device. That is, it is important to remember when calculating R_m (as well as C_m, R_s, and C_s) that the voltage dependence of C_f be remembered and that this dependence reflected in the subsequent calculation. In order to determine the value of $C_f(V)$, a plot of the Spline generated approximate fast capacitance can be examined for the voltage level in question (see Fig. 6.17). However, for the modeling procedure outlined, the voltage level most likely will not decrease significantly during the time periods of interest and for many models, the value found for $C_{f,final}$ can be used as an approximation of $C_f(V)$ for the calculation of R_m (as well as C_m, R_s, and C_s).

$$R_m \cong \frac{V_t \mid_{t=t_{x1}}}{C_f(\frac{dV_t}{dt})} \tag{6.8}$$

Using (6.8) and the procedure outline in Chapter 3, the value of R_m was calculated as ~93.49 mΩ.

$$R_m = \frac{2.20\ V}{588.3\ F \times (\frac{0.004\ V}{1\ s})} = 93.49\ m\Omega$$

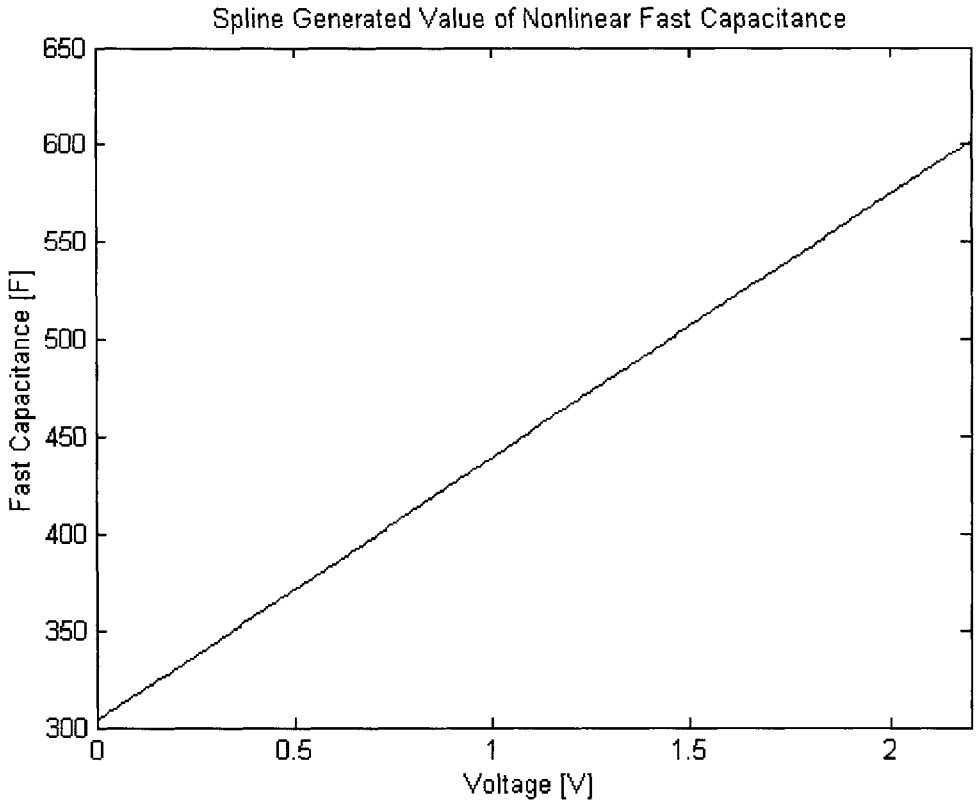

Figure 6.17: Spline Generated Nonlinear Capacitance

6.4.3 Calculation of C_m

The value of C_m is calculated by looking at the measured voltage data following a short interval after the current source is removed and following the extraction procedure of Chapter 3.

	Maxwell 450 F DLC
$C_{f,initial}$	411.8 F
$C_{f,final}$	588.3 F

Table 6.2: Voltage dependent capacitance for C_f

Equation 6.9 shows the equation for calculating C_m (as derived in Chapter 3). The value of $C_f(V)$ is approximated as $C_{f,final}$ as the voltage has changed relatively little since the calculation of $C_{f,final}$.

$$C_m \cong \frac{\Delta Q_2}{V_{C_f|t=t_6} - C_f \frac{dV_t}{dt}|_{t=t_6} (R_m)} \tag{6.9}$$

Using these procedure of Chapter 3 and (6.9), the value of C_m is calculated as ~29.03 F.

$$C_m = \frac{58.83 \text{ C}}{2.12 \text{ V} - 588.3 \text{ F} \times (\frac{0.005 \text{ V}}{30 \text{ s}}) \times (95.4 \text{ m}\Omega)} = 29.03 \text{ F}$$

6.4.4 Other Model Parameters

The remaining model parameters were calculated following the procedure outlined in Chapter 3 and by using the approximated value of $C_f(V)$. These parameters are shown below. Table 6.2 gives the range of values for C_f.

$$R_f = 1.88 \text{ m}\Omega$$

$$R_s = 4.054 \ \Omega$$

$$C_s = 73.5 \text{ F}$$

	Maxwell 450 F DLC		
	Resistance (Ω)	*Capacitance* (Farad)	*Time Constant* (second)
Fast	0.00188	411.8 $\rightarrow$ 588.3	0.77 $\rightarrow$ 1.11
Medium	0.09349	29.03	2.71
Slow	4.05	73.5	297.68

Table 6.3: Extracted Parameters for the 450 F Maxwell DLC Model

6.4.5 Extracted Model

Figure 6.18 shows the six model parameters extracted in the above example. Table 6.3 summarizes the parameters of each of the branches and their respective time constants. As can be seen from the results of this extraction exercise presented in Table 6.3, several assumptions made previously have been validated (as presented in Chapter 3 and earlier in this Chapter). Equation 6.3 stated that the resistance of the fast branch was much less than the resistance of the medium and slow branches and that the resistance of the medium branch is much less than the resistance of the slow branch. Additionally, (3.4) assumed that the resistance of the fast branch could be approximated as zero in some cases when using this procedure. We see from Table 6.3 that relative to the other resistances in the model, the fast branch resistance can be approximated as zero in some cases which allows the resistance of that branch to be neglected in some calculations and allows the statement that $V_t \cong V_{C_f}$ to be made in those cases. And finally, (6.2) states that the time constant of the fast branch was much less than the time constants of the medium and slow branches and that the time constant of the medium branch is much less than the time constant of the slow branch. The question now remains as to the performance of the model with respect to the device performance.

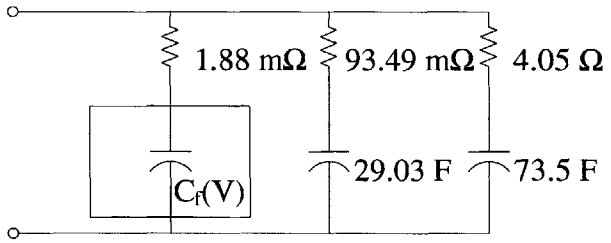

Figure 6.18: Extracted Parameters for the 450 F Maxwell DLC Model

6.4.6 Comparison of Simulated Model to Experimental Data

This subsection gives a comparison of experimental device performance with the DLC model derived above. Using the Matlab®, the DLC model was simulated under conditions similar to that in the lab with the actual device.

As can be seen in Fig. 6.19, the performance of the model tracks the performance of the device extremely well. Both curves demonstrate an initial jump in voltage due to the Thévenin resistance ($R_{Thevenin} \cong R_f$) of the device and model, and a nonlinear rise in voltage to ~2.34 V. The values (voltage) of both curves drop once the current source is removed and continues to slowly decrease in time.

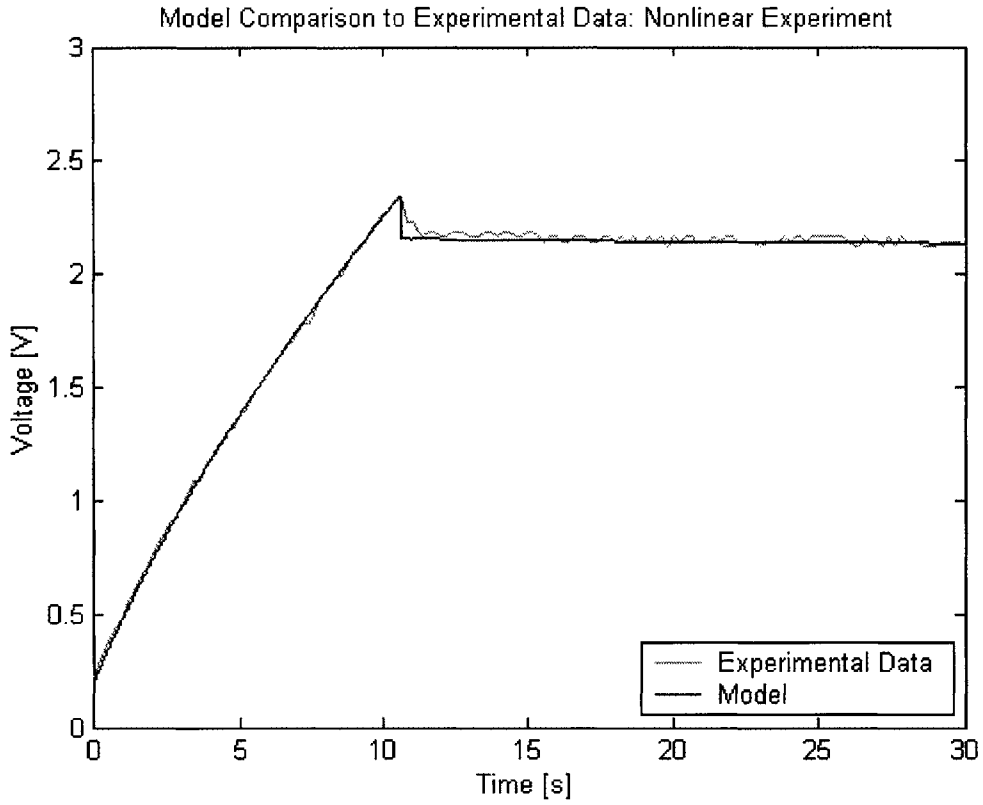

Figure 6.19: Model Comparison for 450 F Maxwell DLC (0 to 30 s)

Looking on the time scale of 0 to 300 s (Fig. 6.20), the performance of the model is very good when compared to the performance of the device. Both curves are in very good agreement as the voltage decreases, especially from 0 to ~200 s.

Figure 6.21 shows the performance of the model and device from 0 to 3000 s. The model shows fair agreement with the performance of the device. The model parameters obtained for these simulations were not adjusted as they were for the model used in Chapter 4. They were obtained by following the modeling procedure presented in Chapter 3 with only the C_f calculation substituted by the procedure presented in this chapter.

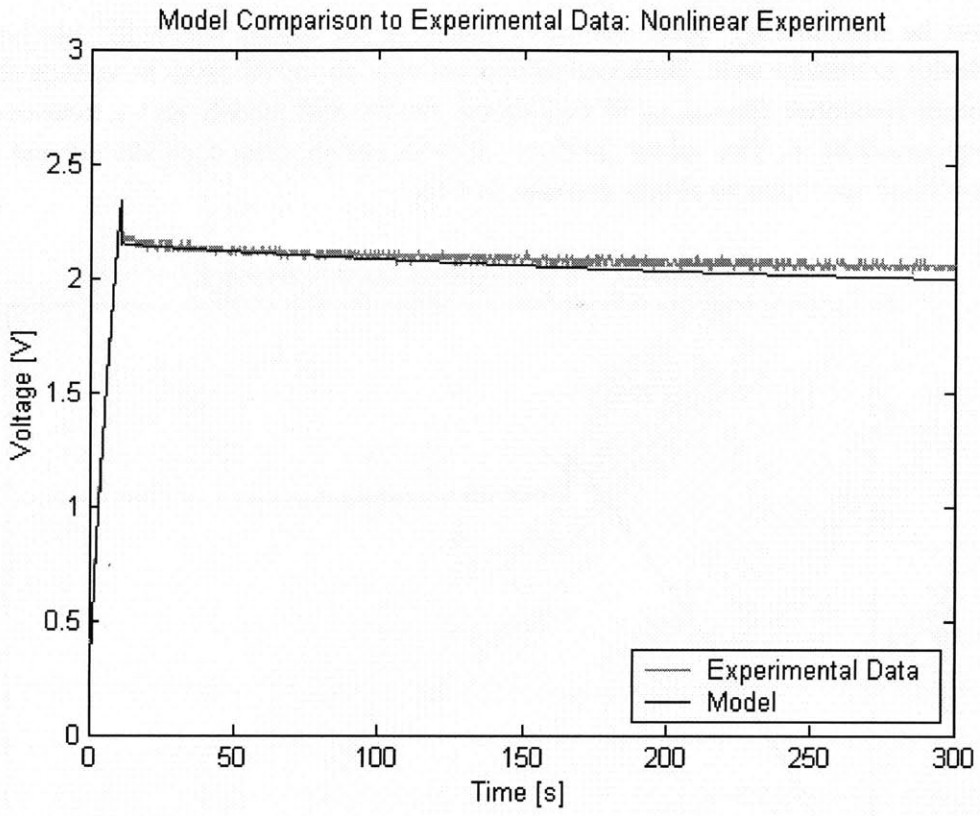

Figure 6.20: Model Comparison for 450 F Maxwell DLC (0 to 300 s)

6.5 Conclusion

In conclusion, the extraction exercise covered in this section has resulted in a six parameter model of a DLC. Upon analyzing this model, many of the assumptions pertaining to the model parameters (resistance, capacitances, and time constants) have been confirmed. Additionally, Figs. 6.19 - 6.21 demonstrate that the model performs very well when simulating the performance of the device. Finally, the nonlinearity seen when charging the device (see Fig. 6.3) is modeled very well with procedure. The use of this modeling procedure and the Spline function of Matlab® results in a fairly accurate and easy to derive DLC model.

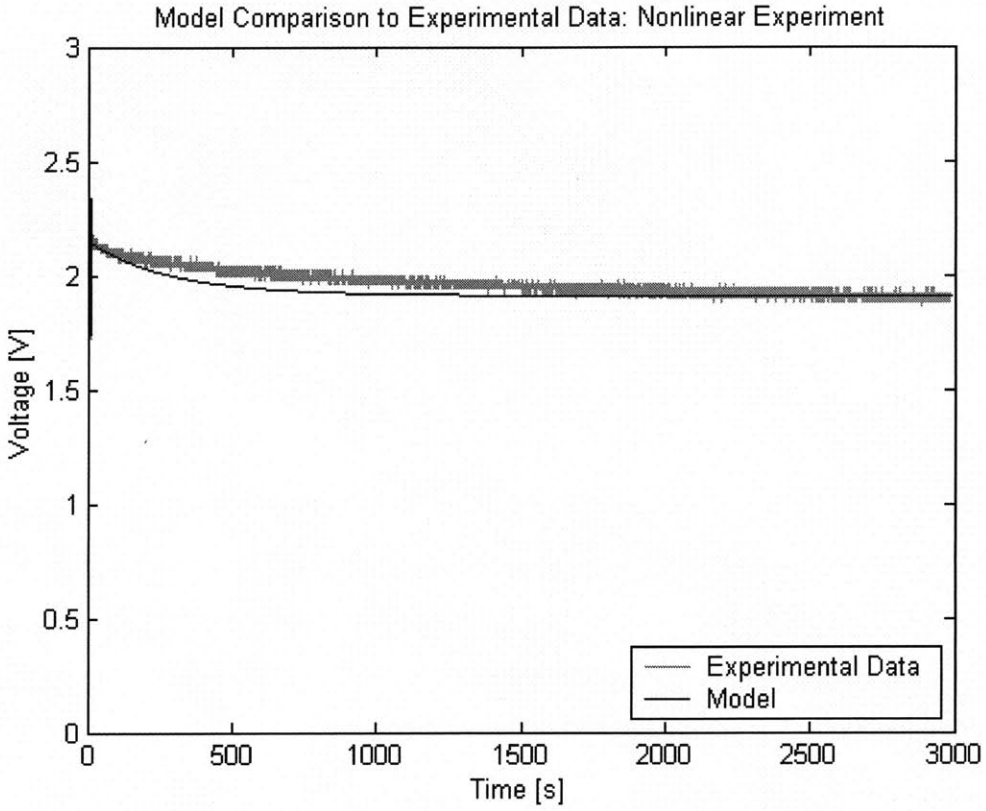

Figure 6.21: Model Comparison for 450 F Maxwell DLC (0 to 3000 s)

Chapter 7

An Investigation of Device Variances

7.1 Introduction

A main advantage of double layer capacitors over many other capacitor technologies is that these devices have much higher capacitances (and thus energy storage capabilities) per unit volume (or weight). However, variations in the device's capacitance can have a large impact on the electrical system of which these devices are a part.

Consider the following example using a hypothetical DLC device with a capacitance of 1000 F (±10%) and a maximum rated voltage of 2.5 V. Now, consider that three of these devices are connected in series, charged with a constant current source of 225 A for 10 s so that the 1000 F ("rated" capacitance) device would charge to 2.25 V (assuming a constant charging profile), well below the maximum device voltage . Furthermore, the actual (measured) capacitance of these three devices are 900 F (representing a lower limit of the capacitance specification), 1000 F, and 1100 F (representing an upper limit of the capacitance specification) respectively. Figure 7.1 illustrates the example of these three devices connected in series and being charged by a constant current source. Using the relation of (7.1), assuming a constant charging profile (i.e., neglecting the nonlinearity of these devices presented in Chapter 6), and storing 2250 C of charge (i.e., 225 A of constant current for 10 s), the three devices would charge to 2.5 V, 2.25 V, and 2.05 V respectively.

$$\mathrm{C} = \frac{\Delta Q}{\Delta \mathrm{V}} = \frac{I\Delta \mathrm{t}}{\Delta \mathrm{V}} \tag{7.1}$$

There are several concerns in a situation like this. In the above example, the safety margin used in charging these devices (i.e., charging to 90% of the maximum voltage) was barely adequate in this case and device is in danger of being overcharged. Next, the three devices will all exhibit different discharge currents/rates (assuming matched leakage resistances). And finally, the voltage of the DLC bank (the series connection of multiple DLCs) may exceed or fall short of the expected bank voltage, depending on the actual capacitances of the devices in the DLC bank. In the above example, the bank voltage would measure 6.8 V

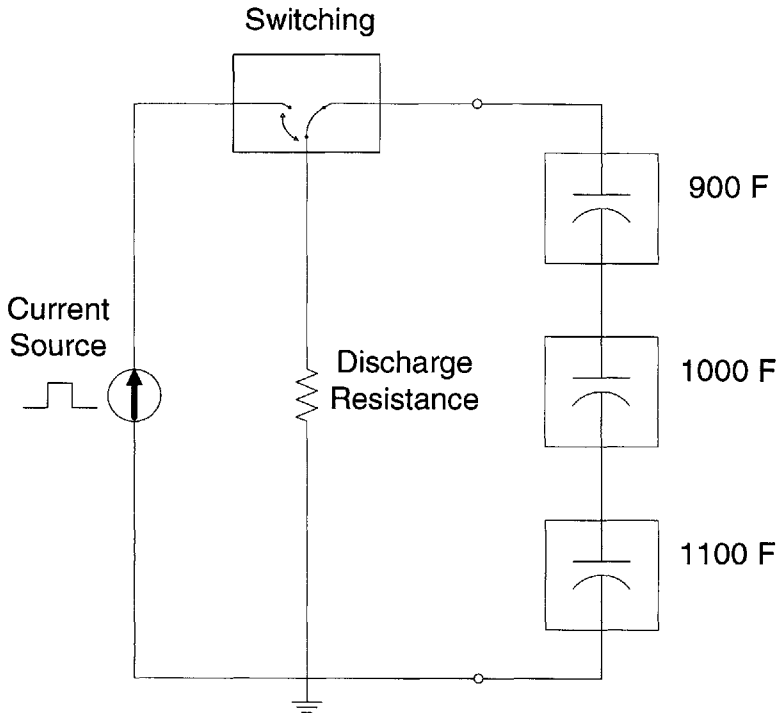

Figure 7.1: Series Connected DLC Circuit

(2.5 V + 2.25 V + 2.05 V) instead of the expected 6.75 V (2.25 V + 2.25 V + 2.25 V) of a bank consisting of three 1000 F (actual capacitance) devices. In this example, the variation in bank voltage is not very great due to the chosen device variations. However, consider a DLC bank of 20 DLCs (using our hypothetical device outlined above) as would be used in a 42 V advanced automotive electrical system. In this example, the devices are charged with 225 A for 10 s so that each device should measure 2.25 V resulting in a bank voltage of 45 V. In this example, the actual capacitance of the 20 devices is found to be 900 F (the lower limit of our capacitance specification) and the resulting bank voltage (assuming a linear charging profile) is found to be 50 V (2.5 V per device). Using a bank consisting of "upper" limit device (i.e, devices with an actual capacitance of 1100 F) would result in a bank voltage of 41 V.

The capacitance variation of our hypothetical device discussed above was modestly chosen for these examples. However, the variations specified by the manufacturer are often much greater. NessCap specifies a variation of (-10%/+30%) for their devices, while Maxwell specifies a variation of (±20%). These possibly large variations in the device's capacitance are cause for concern. In an effort to investigate the current variation in manufactured device, a Variation Experiment was setup and performed. For this experiment, six 450 F, 2.5 V devices were ordered from Maxwell and connected in series as shown in Fig. 7.2. The

devices were then charged with a constant current source for a short time period while the terminal voltage of the six devices was observed.

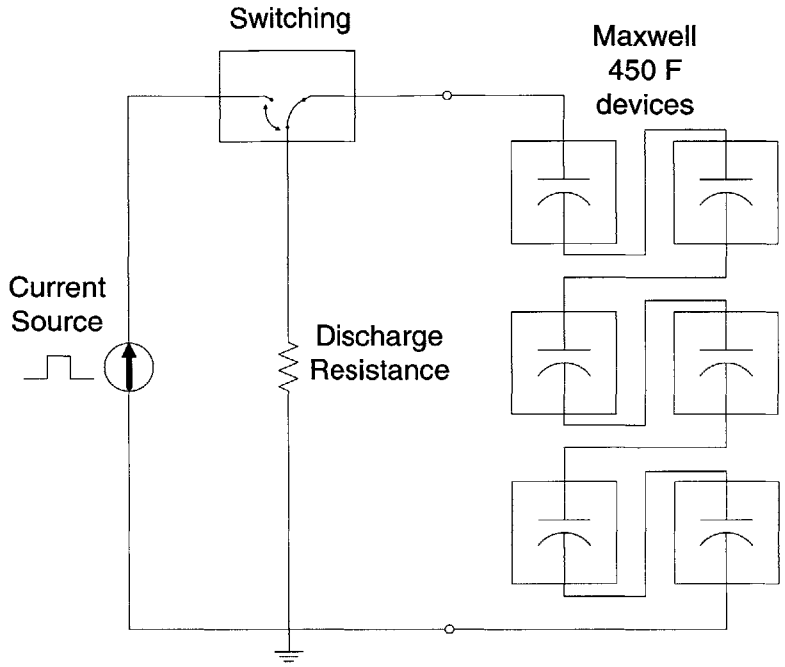

Figure 7.2: Experimental Circuit of Series Connected DLCs

7.2 Test Setup

A diagram of the test circuit for the "variance experiment" is shown in Fig. 7.3. The test circuit consist of two TDS 745 oscilloscopes (each of which have 4 channels), two HP 6011A power supplies (set to operate as constant current sources), two AM 503B current amplifiers (with A6303 current probes), a three position mechanical switch, a discharge resistance, a "diode circuit," the "differential amplifier board" (the board consist of the six INA105 differential amplifiers shown in Fig. 7.3 and additional circuitry to support the board, not shown in Fig. 7.3), a power supply for the differential amplifier board (not shown in Fig. 7.3), and six 450 F Maxwell DLCs connected in series. Figure 7.3 illustrates that the DLC "cluster" is charged with two current sources through a diode circuit. The diode circuit is shown in Fig. 7.4. This circuit consist of four IR 83CNQ080A diodes and is used as a precautionary measure to prevent the current flowing from on current source into the other. Two of the 80 A diodes are paired in parallel to handle the charging current supplied by each current source (which in some experiments is ~100 A). Current measurements for the circuit are made by the A6303 current probes. Each current probe is rated at ~100

A. This particular experiment used a charging current of ~150 A (75 A from each of the two current sources). The current probes were placed on the line supplying the charging current at the current source (i.e., before the diode circuit) for the current measurements. The signals from the current probes where fed to the AM 503B current amplifier and then to the oscilloscope (channels 3 & 4 of the oscilloscope).

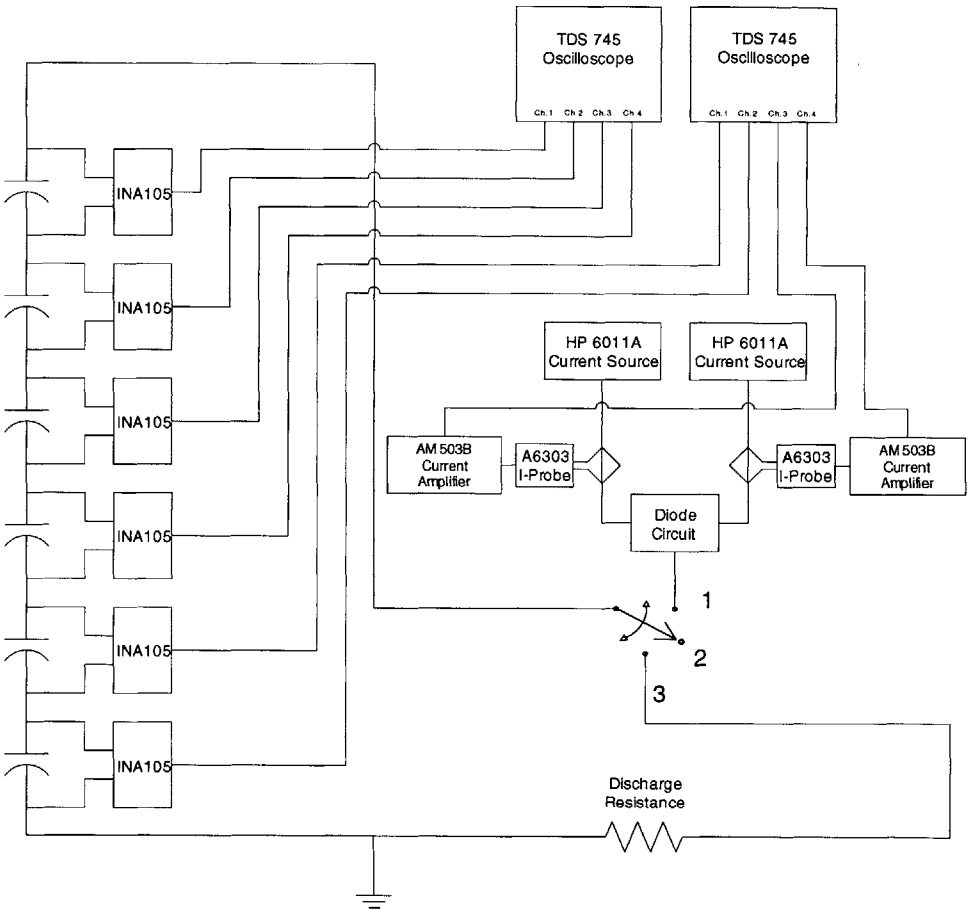

Figure 7.3: Variance Experimental Test Setup

Figure 7.5 shows a detailed view of the DLC cluster and the "interface board." The cluster receives positive current from the 2-AWG wire connected to DLC #1. The current flows through the series connection of DLCs, leaving the cluster at DLC #6. The six DLCs are connected in series by six large copper buss bars and the cluster is mounted on a plexiglass floor. The terminal voltage of each device is measured by six of the eight channels of the two oscilloscopes (channels 1 thru 4 of one oscilloscope, and channels 1 & 2 of the second oscilloscope). As in the previous experiments, copper foil was placed in the terminals of the device, held in place by a stainless steel lug. The lug also provides a mechanical connection to the buss bars and an electrical connection throughout the circuit. The voltage signal on

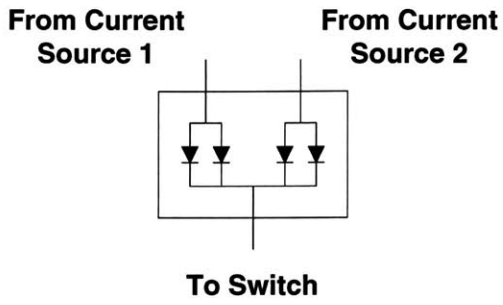

Figure 7.4: Diode "Or" Circuit

the copper foil is run to the interface board where it may be observed by the oscilloscopes through a convenient BNC connection. Figure 7.6 shows a detailed view of the interface board and its seven BNC connectors. Six of the BNC connectors are used to measure the individual voltage of the six DLCs in the cluster, while the seventh BNC connector provides a measurement of the series combination of devices.

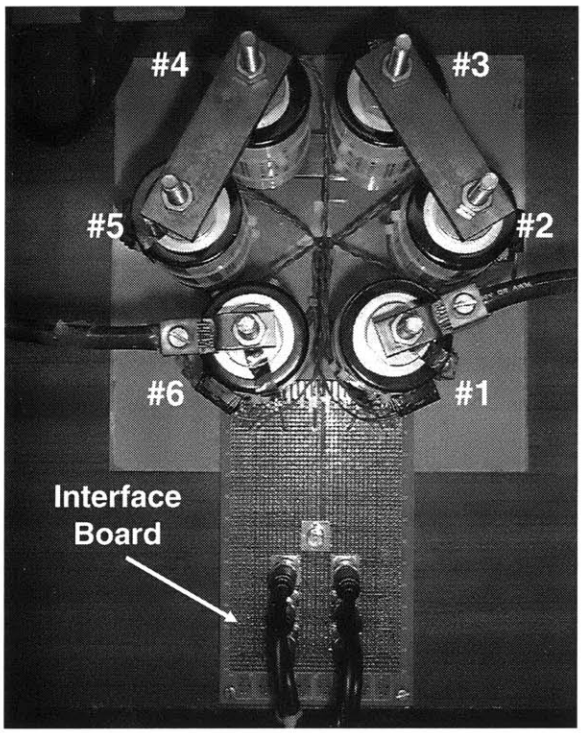

Figure 7.5: DLC Cluster and Interface Board

A differential amplifier board was assembled to allow the measurement of the six voltage signals from the device cluster. The precision unity gain INA105 differential amplifier (shown in Fig. 7.7) was selected for the task due to its high input impedance (50 kΩ) and

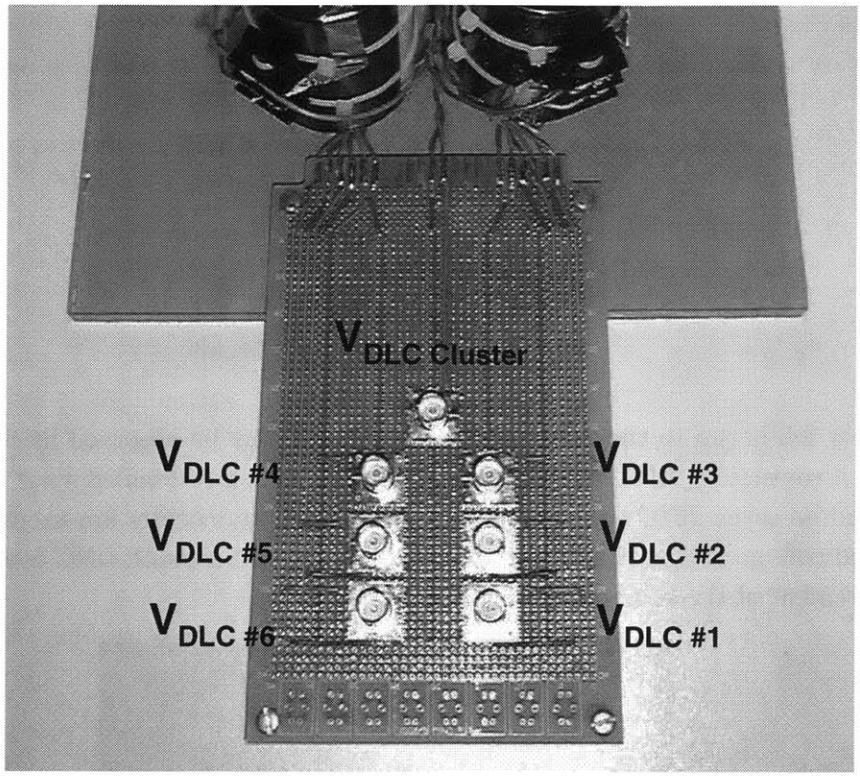

Figure 7.6: Interface Board

its low gain error (0.01% max). A low gain error was required for the differential amplifier circuit so as to minimize the error in the "measured" voltage. Six of these differential amplifier circuits were used and mounted to the differential amplifier board shown in Fig. 7.8.

Figures 7.9 & 7.10 show the test circuit in the laboratory. Figure 7.9 illustrates the two oscilloscopes, the two current sources, the power supply for the differential amplifier board, the differential amplifier board, the current amplifiers, and the DLC cluster with interface board. Figure 7.10 gives a detailed view of the test setup centered around the DLC cluster.

The testing procedure for this experiment was similar to that used in the modeling procedure presented in Chapter 3. The series combination of devices were charged with a constant current of ~150 A until the voltage of the devices reached ~2.25 V. A multimeter was used to measure the voltage of one of the devices (DLC #1) while charging, so that its voltage could be observed in real time. A maximum charging voltage of 2.25 V (for DLC #1) was chosen so as to avoid over-voltaging the devices. The capacitance of DLC #1 was investigated prior to this experiment; the capacitance of this device was determined to correspond closely to the rated capacitance of that device (i.e., this device's capacitance was

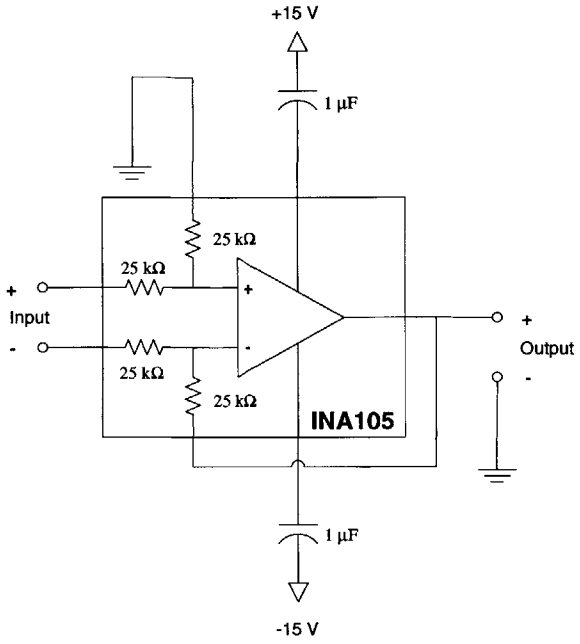

Figure 7.7: Precision Unity Gain Differential Amplifier Circuit

not found to be at the extremes of the manufactures variance specification). It was assumed that the capacitance rating of the six devices would be similar enough that once DLC #1 reached ~2.25 V that DLCs #2 - 6 would not exceed 2.5 V (the maximum continuous operating voltage of the DLC). Once DLC #1 was charged to ~2.25 V, the mechanical switch was moved to the "2" position (seen in Fig. 7.3) to open-circuit the device cluster for the remainder of the experiment.

7.3 Experimental Results

For this experiment, the initially discharged device received a pulse of constant current until the device voltage reached ~2.25 V. The current source was then removed and the device open circuited for the remainder of the experiment. With the experiment complete, the data was collected and examined. Figure 7.11 shows the $v(t)$ curves for the six devices on the time scale of 0 to 6 s. As can be seen from this figure, there is a small variation in the maximum voltage attained by each device. This variation is about 0.1 V (DLC #2 reached ~2.04 V while DLC #3 reached ~2.14 V). Devices #2 & 3 have exhibited the extremes in terms of performance as compared to the six device, while the performance of devices #1 & #4 - 6 fall in between that of devices #2 & 3.

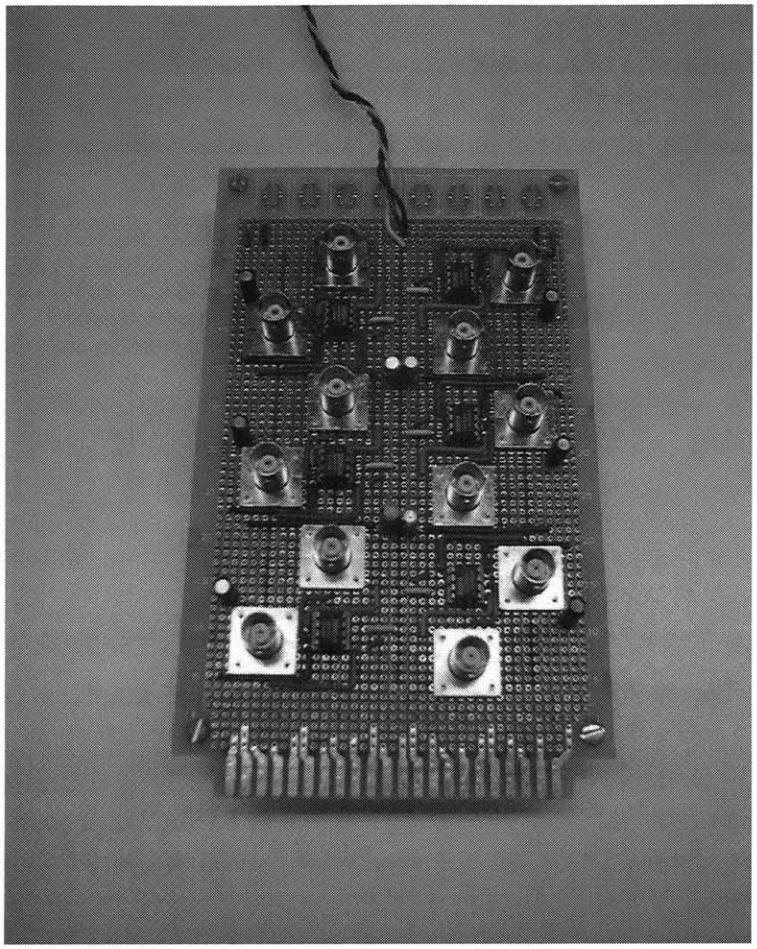

Figure 7.8: Differential Amplifier Board

Figure 7.12 illustrates the time scale of 0 to 30 s. In this figure, DLC #3 is seen to maintain the highest voltage during this interval, while DLC #2 maintains the lowest. The other four $v(t)$ curves fall in between that of device #2 & #3 as in the previous plot. Figures 7.13 & 7.14 show the $v(t)$ curves for the extended time scales of 0 to 300 s and 0 to 3000 s respectively.

Figure 7.15 gives a plot of the two "extreme" devices (DLC #2 & DLC #3). The time scale for this plot is 0 to 30 s. Figures 7.16 & 7.17 illustrate the extended time scales of the performance of these two devices. As can be seen in Fig. 7.17, the ending voltage of DLC #2 is $\sim$1.58 V while the ending voltage of DLC #3 is $\sim$0.12 V higher at $\sim$1.70 V.

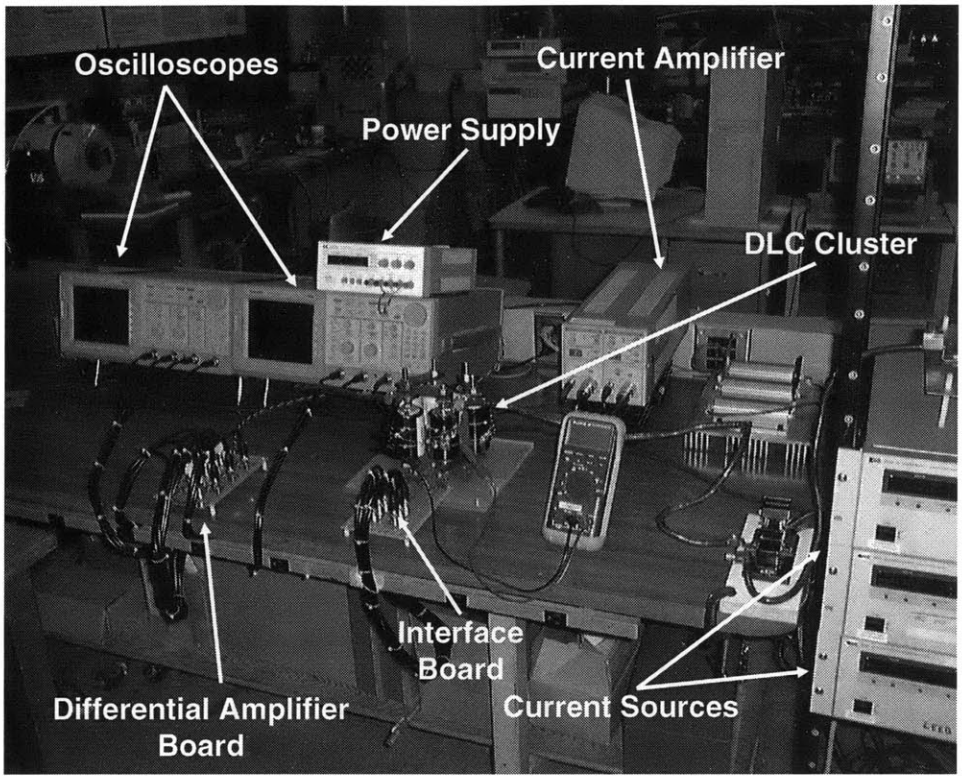

Figure 7.9: Laboratory Test Setup

7.4 DLC Models & Extraction Calculations

The modeling procedure used for this experiment was the same as that presented in Chapter 6. In an effort to investigate the variances in capacitance, the modeling procedure was preformed on devices #2 & #3 (as these devices gave an outer boundary, with all the other devices falling within those bounds) rather than all six devices. Furthermore, the comparison of the device models will be limited to a comparison of the fast branch parameters (R_f and the nonlinear capacitance, $C_f(V)$) and the device performance during the charging of the device. That is, the devices will be compared over the region of operation that they would be used for in power electronics type applications (rather than as long term energy storage applications) and their fast branch capacitance (nonlinear as a function of voltage) will be compared.

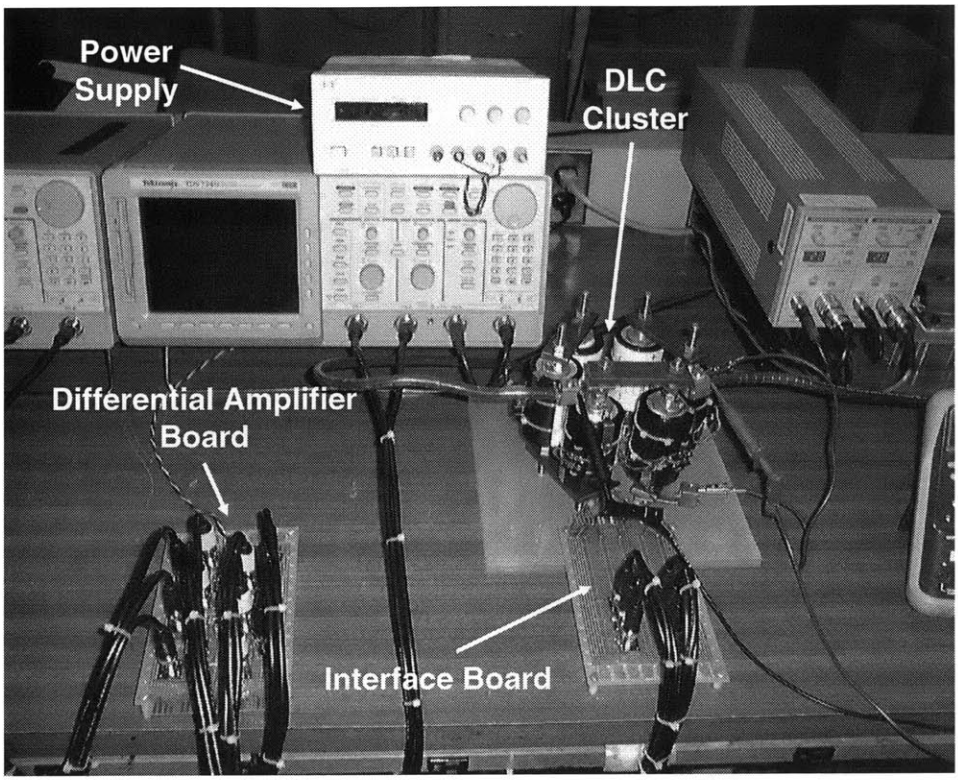

Figure 7.10: Laboratory Test Setup

7.4.1 DLC #2

The calculation of R_f follows (7.2). The device was charged with constant current of ~150 A, but due to the overshoot by the source at the onset of the current, a value of 192 A is used in the calculation of the ESR (which is approximately equal to R_f). An example of the overshoot of current produced by the current source can be seen by reviewing the i(t) waveform shown in Fig. 6.14. The initial jump in the v(t) waveform (during which the device received ~192 A of current) was found to be ~0.34 V. An example of a v(t) waveform that illustrates the "initial jump" in voltage can be found by reviewing the waveform illustrated in Fig. 6.16. Using (7.2) and the measured values of ΔV and ΔI, the calculated value of the device's ESR is found to be approximately 1.77 mΩ. This value of R_f is in the range expected, as the value found for device #1 in section 6.4.4 of Chapter 6 was approximately 1.88 mΩ.

$$R_f = \frac{\Delta V_t}{\Delta I} \tag{7.2}$$

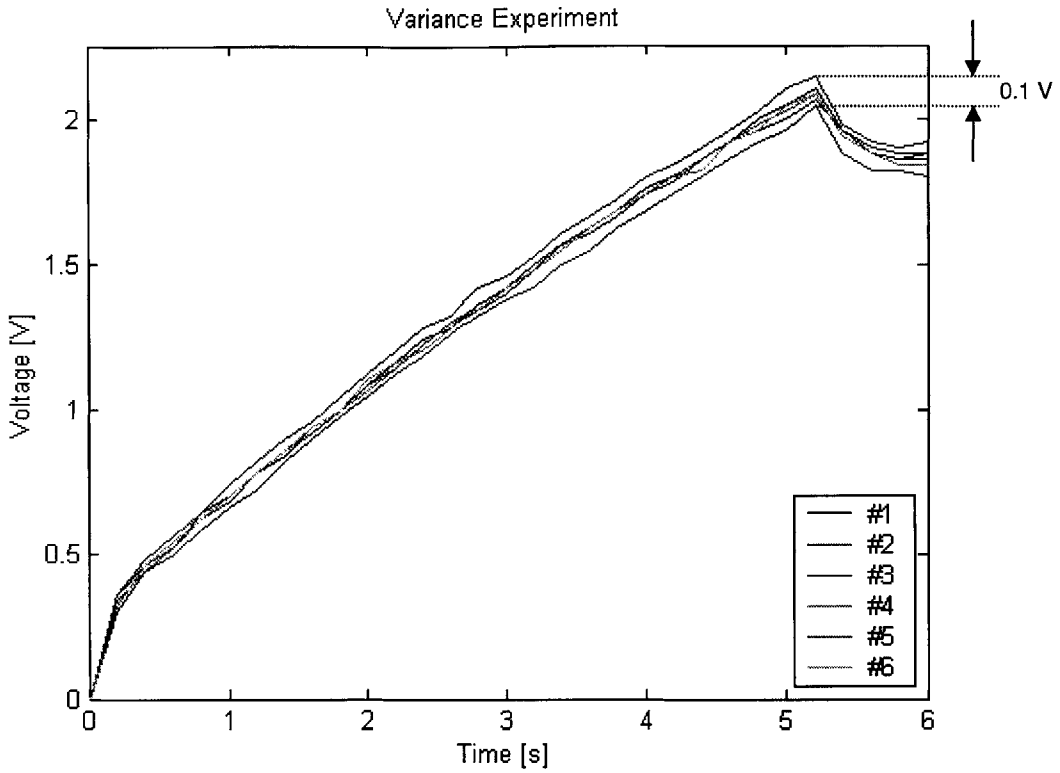

Figure 7.11: DLC Voltage Curves (0 to 6 s)

$$R_f = \frac{\Delta V_t}{\Delta I} = \frac{0.34\ \text{V}}{192\ \text{A}} = 1.77\ \text{m}\Omega$$

The calculation of the nonlinear capacitance, $C_f(V)$, follows the method presented in Chapter 6. An initial and a final capacitance (each with an associated voltage level of C_f) was determined by investigating the device's response to a constant current (approximately constant since there is an initial overshoot) over an interval. In Chapter 6, the charging interval was approximately 11 s and the initial interval and final interval used to calculate the initial and final capacitance was chosen as 3 s. This interval was chosen as short enough that the change in voltage could be approximated as nearly linear, but long enough that the calculation could easily be made without being effected by noise in the data. For the variation experiment, the charging interval was approximately 5 s. Initially, a 1 s interval was chosen for the calculations of $C_{f,initial}$ and $C_{f,final}$. However, the noise in the data provided capacitance values much too high for this device. The interval of 2 s was then chosen for the calculations. More reasonable values of $C_f(V)$ were then obtained. Equation 7.3 gives the relation for $C_{f,initial}$, while (7.4) is used to find $\Delta Q_{initial}$. At the beginning

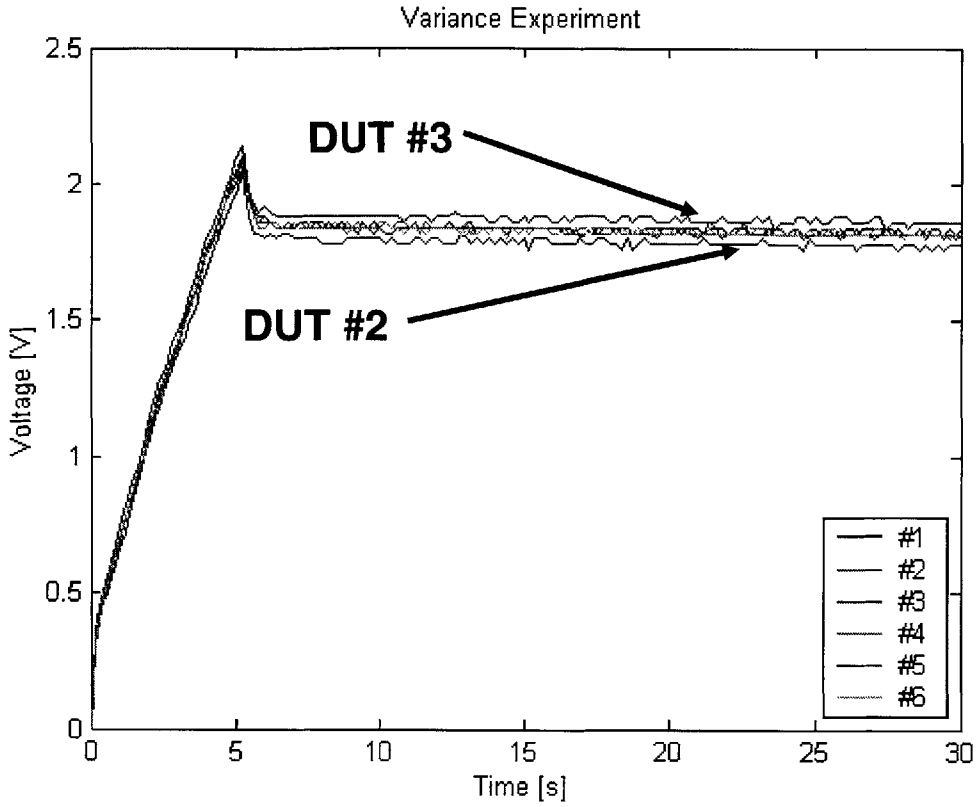

Figure 7.12: DLC Voltage Curves (0 to 30 s)

of the 2 s interval, the device's terminal voltage (and therefor the voltage of C_f) was 0 V. At the end of the 2 s interval, the device's terminal voltage was ~0.82 V above the value measured for the initial jump in voltage. Assuming that the entire current flowing into the device during this interval is being stored in the fast branch, the terminal voltage of the device would equal the sum of the voltage across C_f and the initial jump in the $v(t)$ waveform (which would equal the voltage drop across R_f). The value for $C_{f,initial}$ was found to be 423.8 F with an associated voltage level of 0.82 V.

$$C_{f,initial} = \frac{\Delta Q_{initial}}{\Delta V_{t,initial}} \tag{7.3}$$

$$\Delta Q_{initial} = \int_0^{t=2s} i(t)dt \cong \Sigma(I \times \Delta t) \tag{7.4}$$

$$\Delta Q_{initial} = 347.52 \text{ C}$$

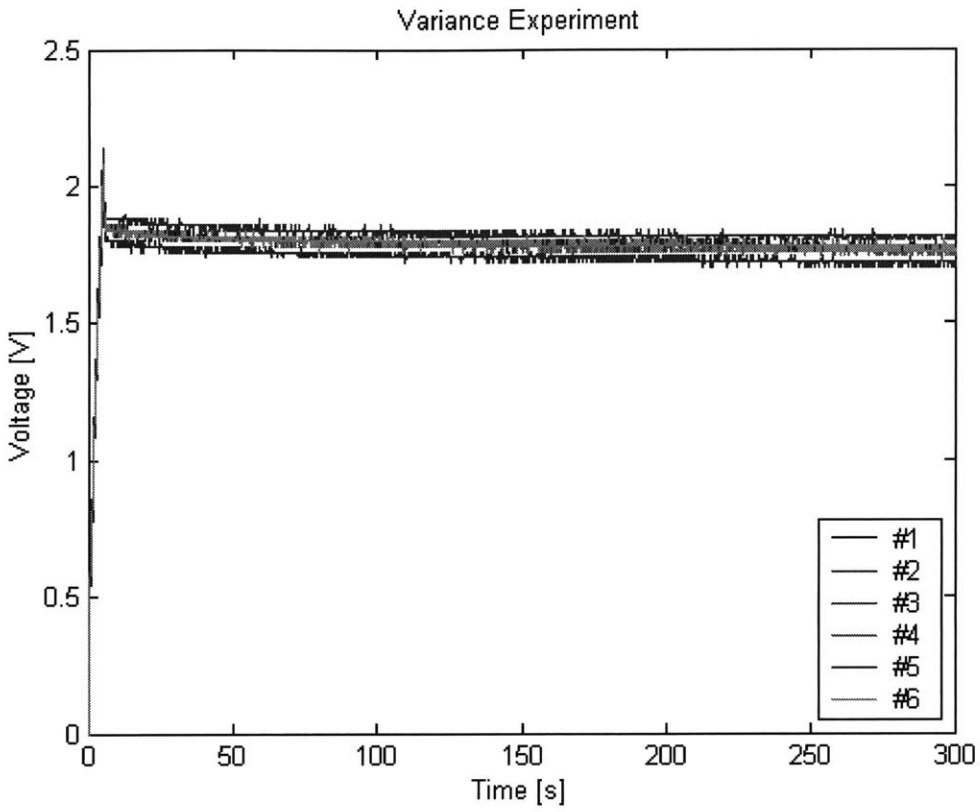

Figure 7.13: DLC Voltage Curves (0 to 300 s)

$$C_{f,inititial} = \frac{\Delta Q_{initial}}{\Delta V_{t,initial}} = \frac{347.52\ C}{0.82\ V} = 423.8\ F$$

In calculating the value for $C_{f,final}$, the v(t) and i(t) waveforms were investigated during the final 2 s of the charging interval. Equations 7.5 & 7.6 were used in finding $C_{f,final}$. The charge stored in the device during this interval was found to be approximately 335.04 C and the change in voltage was ~0.62 V. Using (7.5) and (7.6), $C_{f,final}$ was found to be approximately 540.4 F with an associated voltage level of 1.88 V.

As mentioned in Chapter 6, the associated voltage level for the final capacitance is found by looking at the terminal voltage of the device at the instant that the current source is removed (assuming that the interval used for the calculation ends at the end of the charging interval rather than earlier in that interval). This method of looking at the terminal voltage, rather than to subtract the drop across R_f (as done when associating a voltage level for $C_{f,initial}$), is done to best estimate the voltage across C_f at the end of the interval. It makes the assumption there is zero current flowing in the branch at that instant and that there

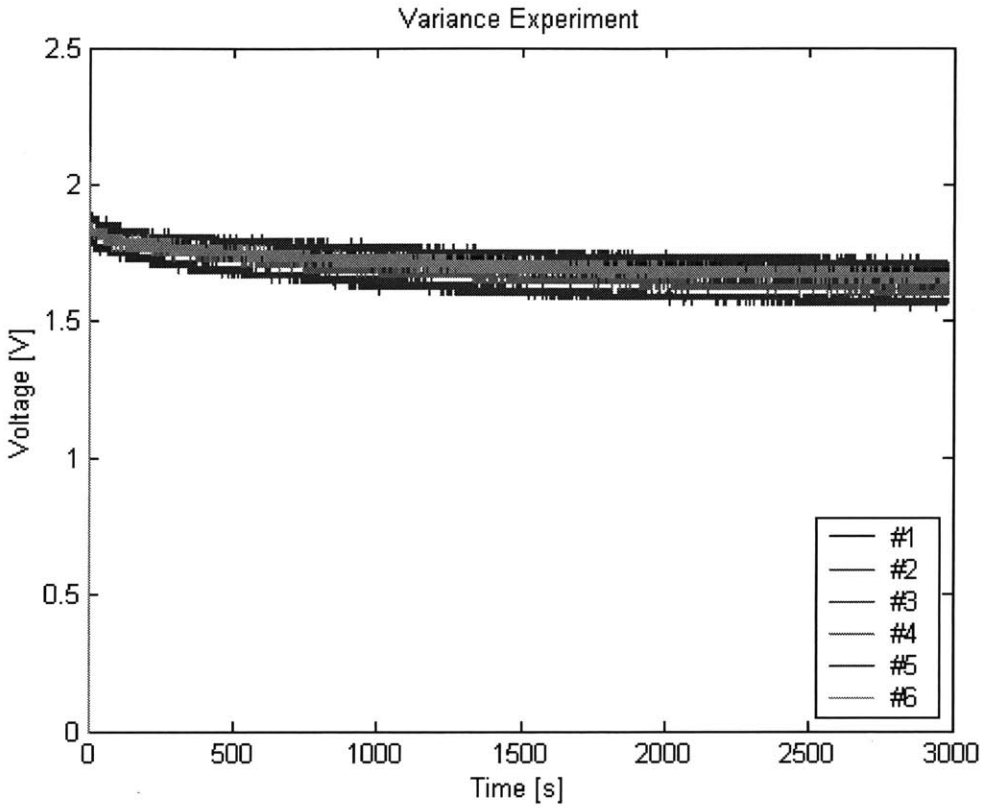

Figure 7.14: DLC Voltage Curves (0 to 3000 s)

is zero voltage across R_f, thus V_t equals V_{C_f} (in reality, a little current will be flowing in the fast branch which will result in a "negative" voltage drop across R_f). Subtracting the drop across across R_f makes the assumption that all the current flowing into the device at the end of the charging interval (and hence for during the entire charging interval) is going entirely into the fast branch. As stated previously, this is a fair assumption when the charging interval is short and the assumption improves as the interval shortens. But in reality, there is some current flowing beyond the fast branch by the end of this charging interval. This is reflected in the fact that the discontinuity at the beginning of the charging interval (the initial "jump" or initial discontinuity) is greater than the discontinuity at the end of the charging interval (once the source is removed). The associated voltage level could also be approximated by subtracting the drop across R_f from the maximum voltage reached at the end of the charging interval instead of using the above mentioned method, but the method used is a better approximation to the voltage level of C_f at that point in time.

$$C_{\text{f,final}} = \frac{\Delta Q_{\text{final}}}{\Delta V_{\text{t,final}}} \tag{7.5}$$

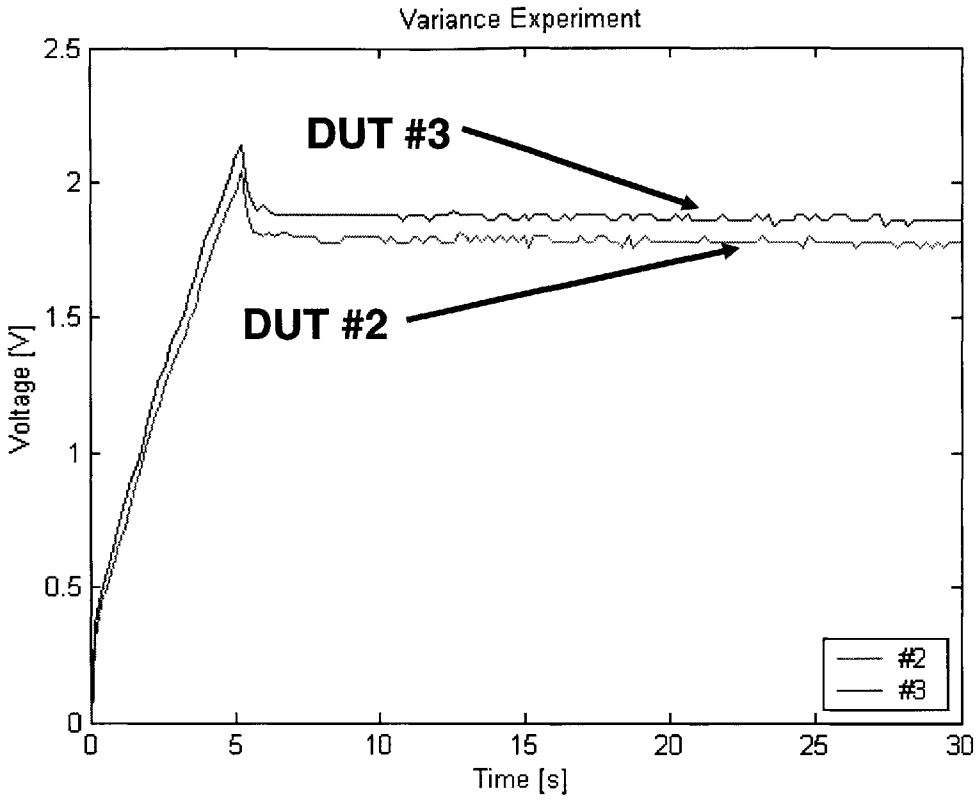

Figure 7.15: DLC Voltage Curves for DLCs #2 & 3 (0 to 30 s)

$$\Delta Q_{final} = \int_{t=3.2s}^{t=5.2s} i(t)dt \cong \Sigma(I \times \Delta t) \tag{7.6}$$

$$\Delta Q_2 = 335.04 \text{ C}$$

$$\mathrm{C_{f,final}} = \frac{\Delta Q_2}{\Delta V_{\mathrm{t,final}}} = \frac{335.04 \text{ C}}{0.62 \text{ V}} = 540.4 \text{ F}$$

Table 7.1 summaries the values of the fast branch parameters for DLC #2. The resistance of the fast branch (approximately the device's ESR) was found to be 1.77 mΩ, while $C_f(V)$ changed from 423.8 F to 540.4 F over the range of 0.82 V to 1.88 V.

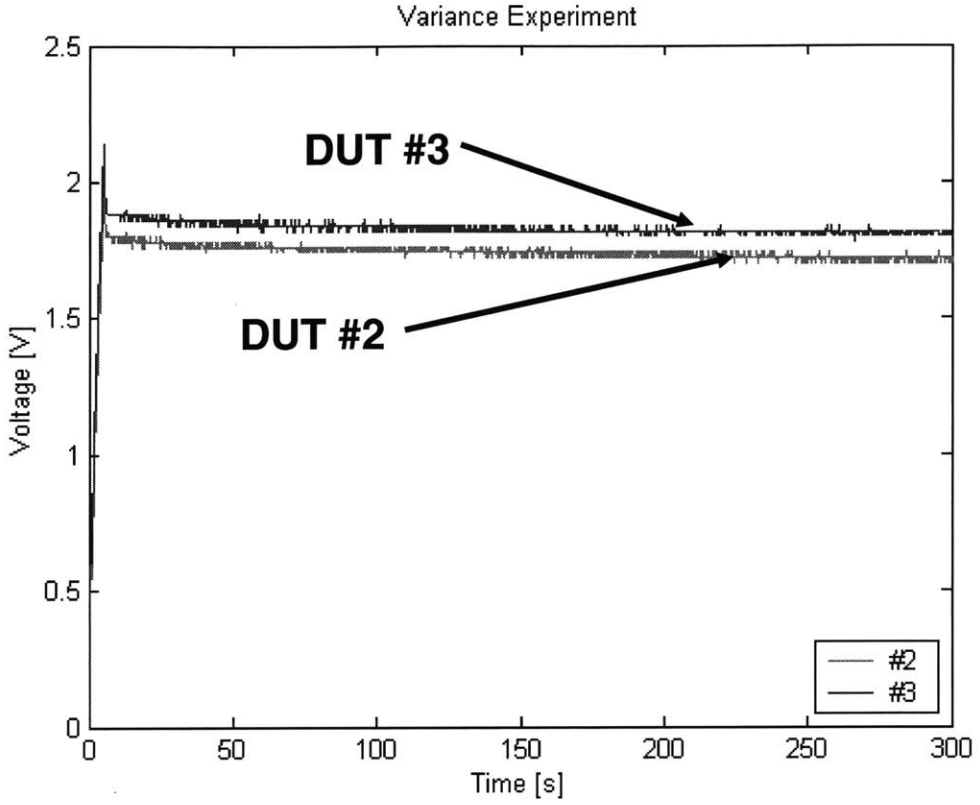

Figure 7.16: DLC Voltage Curves for DLCs #2 & 3 (0 to 300 s)

7.4.2 DLC #3

The calculations of R_f, $C_{f,initial}$, and $C_{f,final}$ are preformed using (7.2), (7.3), and (7.5) respectively and using the 2 s calculation interval mentioned in the previous section. The ESR (and thus our approximated value of R_f) of DLC #3 was found to be 2.08 mΩ. Again, this value is in the range expected for our device as this value is similar to that found for devices #1 (Chapter 6) #2 (section 7.4.1), and it is less than (but in the range of) the "maximum ESR" (which is 2.4 mΩ) specified by the manufacture for this device.

	Maxwell 450 F DLC #2	
	Resistance (Ω)	*Capacitance* (Farad)
Fast	0.00177	423.8 $\rightarrow$ 540.4

Table 7.1: Extracted Parameters for the 450 F Maxwell DLC #2 Model

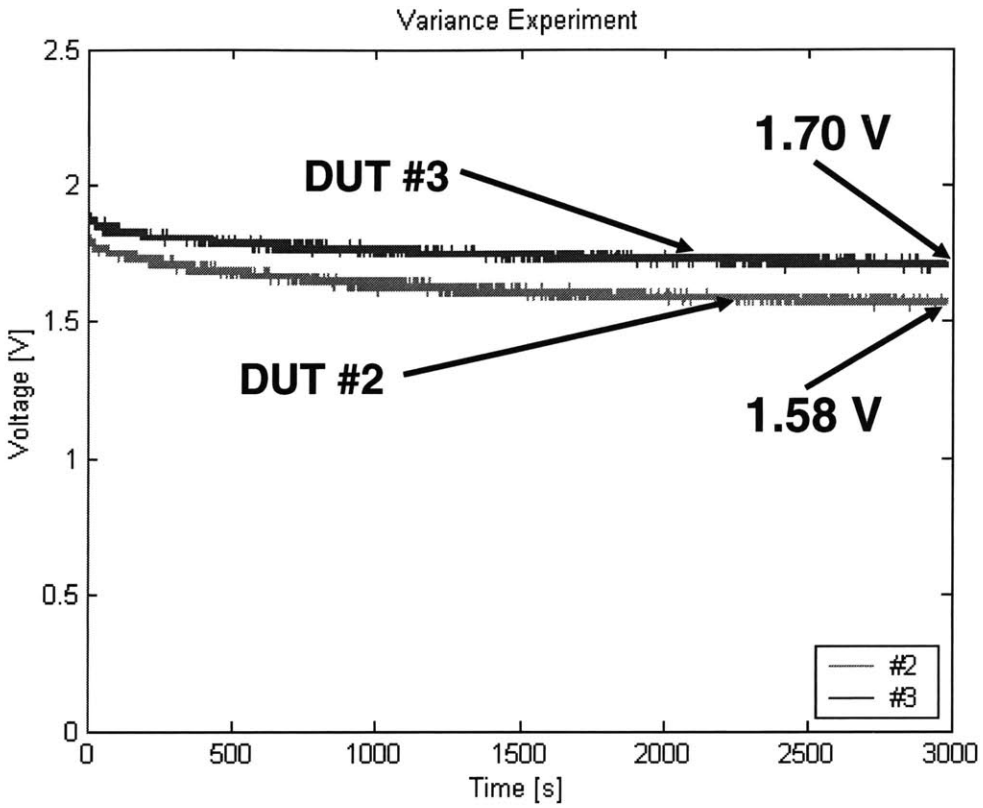

Figure 7.17: DLC Voltage Curves for DLCs #2 & 3 (0 to 3000 s)

$$\mathrm{R_f} = \frac{\Delta V_\mathrm{t}}{\Delta I} = \frac{0.4\ \mathrm{V}}{192\ \mathrm{A}} = 2.08\ \mathrm{m\Omega}$$

The initial capacitance for the this device was found by investigating the initial 2 s of the charging interval. The $v(\mathrm{t})$ curve showed an initial "jump" in voltage once the current source was applied to the device, followed by a nonlinear charging curve. During this short interval, the device's voltage changed by ~0.84 V (ignoring the initial discontinuity in the $v(\mathrm{t})$ curve) while storing 347.52 C of charge. Using (7.3), the device's $\mathrm{C}_{f,initial}$ was found to be approximately 413.7 F at a voltage level of 0.84 V.

$$\mathrm{C_{f,inititial}} = \frac{\Delta Q_\mathrm{initial}}{\Delta V_\mathrm{t,initial}} = \frac{347.52\ \mathrm{C}}{0.84\ \mathrm{V}} = 413.7\ \mathrm{F}$$

The final 2 s of the charging interval were investigated to determine the value for $\mathrm{C}_{f,final}$ and its associated level of voltage. During this interval, the device's terminal voltage changed by

	Maxwell 450 F DLC #3	
	Resistance (Ω)	*Capacitance* (Farad)
Fast	0.00208	413.7 → 540.4

Table 7.2: Extracted Parameters for the 450 F Maxwell DLC #3 Model

Capacitance	*Voltage*
423.8 F	0.82 V
540.4 F	1.88 V

Table 7.3: Data Table for DUT #2

approximately 0.62 V and, therefor the voltage across C_f changed by approximately 0.62 V (assuming a constant R_f and a constant flow of current in the fast branch giving a constant drop across the resistance term in that branch). The device stored 335.04 C during this interval. Using these values and (7.5), the device's $C_{f,final}$ was approximated as 540.4 F at an associated voltage level of 1.98 V.

$$C_{f,final} = \frac{\Delta Q_2}{\Delta V_{t,final}} = \frac{335.04\ C}{0.62\ V} = 540.4\ F$$

Table 7.2 summaries the values of the fast branch parameters for DLC #3. The resistance of the fast branch (approximately the device's ESR) was found to be 2.08 mΩ, while $C_f(V)$ changed from 413.7 F to 540.4 F over the range of 0.84 V to 1.98 V.

7.4.3 "Fast" Branch Variance Comparison

Tables 7.3 and 7.4 provide a comparison of the calculated capacitance parameters (and the associated voltage levels for $C_f(V)$) for DLCs #2 & #3. This table was used when implementing the Spline-based model in Matlab®.

Capacitance	*Voltage*
413.7 F	0.84 V
540.4 F	1.98 V

Table 7.4: Data Table for DUT #3

7.5 Comparison

This section gives a comparison of the DLC models and the experimental data for DLCs #2 & #3. Figure 7.18 plots the $v(t)$ curve for DLC #2 with its model from 0 to 7 s. The model provides a good fit to this experimental data. Figure 7.19 gives the comparison for DLC #3. Again, the model provides a good fit to the data. Finally, the two sets of $v(t)$ curves (experimental data) and their models are plotted in Fig. 7.20.

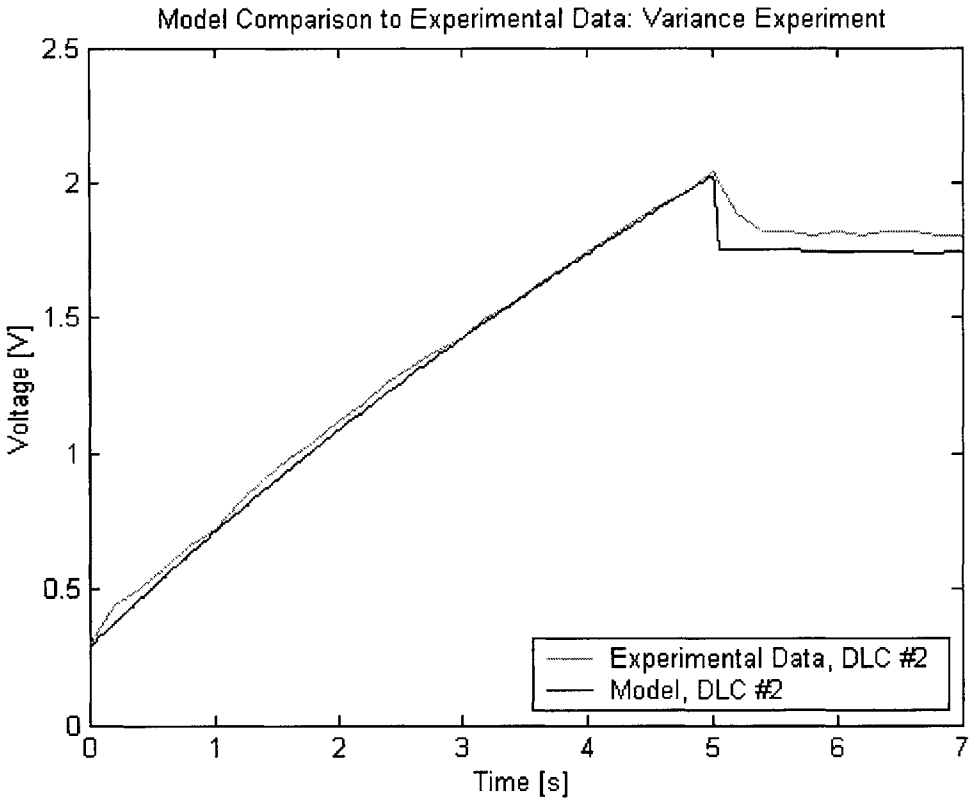

Figure 7.18: DLC #2 vs. Nonlinear DLC Model

A Spline generated plot of the $C_f(V)$ for DLCs #2 & #3 is given in Fig. 7.21. As can be seen from this plot, DLC #2 is shown to have a higher capacitance (for a given level of voltage) than DLC #3. An interesting detail of this plot is that both plots have approximately the same slope (they are nearly parallel) as seen below.

$$\text{slope}_{\text{DLC\#2}} = \frac{C_{f,\text{final}} - C_{f,\text{initial}}}{V_{C,\text{final}} - V_{C,\text{intial}}} = \frac{540.4 - 413.7}{1.88 - 0.82} = 1.10$$

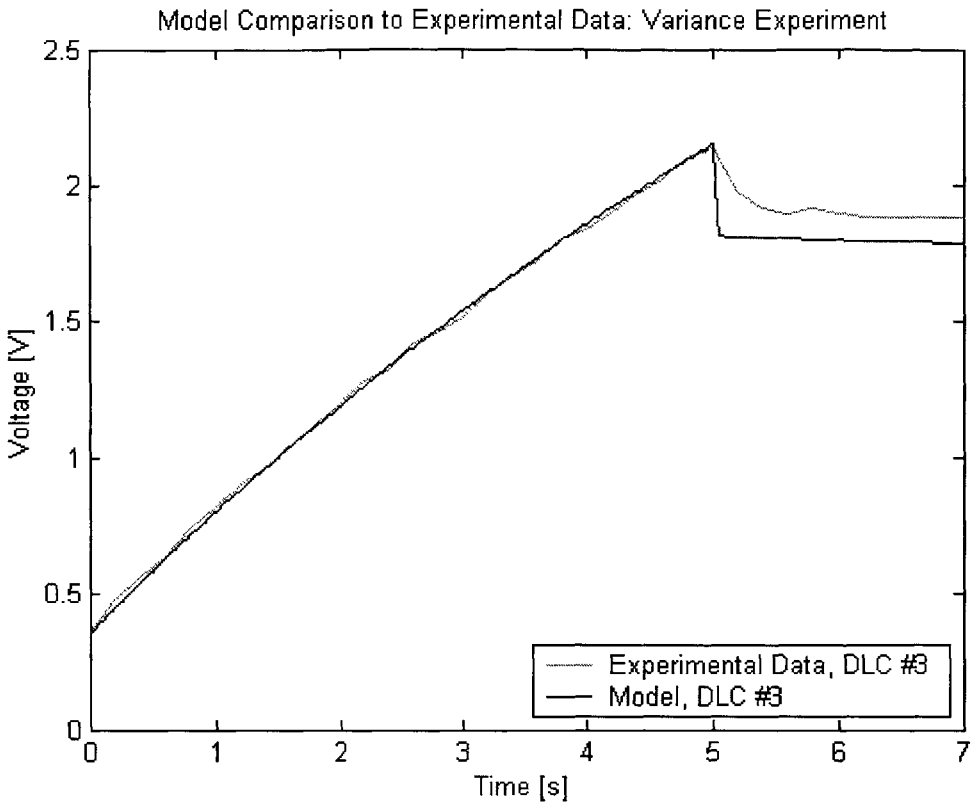

Figure 7.19: DLC #3 vs. Nonlinear DLC Model

$$\text{slope}_{\text{DLC\#3}} = \frac{C_{f,\text{final}} - C_{f,\text{initial}}}{V_{C,\text{final}} - V_{C,\text{intial}}} = \frac{540.4 - 423.8}{1.98 - 0.84} \cong 1.11$$

7.6 Conclusion

An experiment was performed to investigate the device variances in current state-of-the-art manufactured carbon-based DLCs. The concern was that the device variances would be unacceptably high. The variances in capacitance for several lines of DLCs, as stated by the device manufactures, were investigated (see Tables 1 - 3) prior to the experiment. The result of the initial investigation was the belief that the capacitance may vary up to 30% of the specified capacitance rating. However, this experiment has shown that a group of devices (of the same manufcture/model and which were order in a group) obtained and tested did not show the large variance expected. The ESRs of the devices were all lower than that stated as the maximum ESR of the device and were all within 0.3 mΩ of one another. The

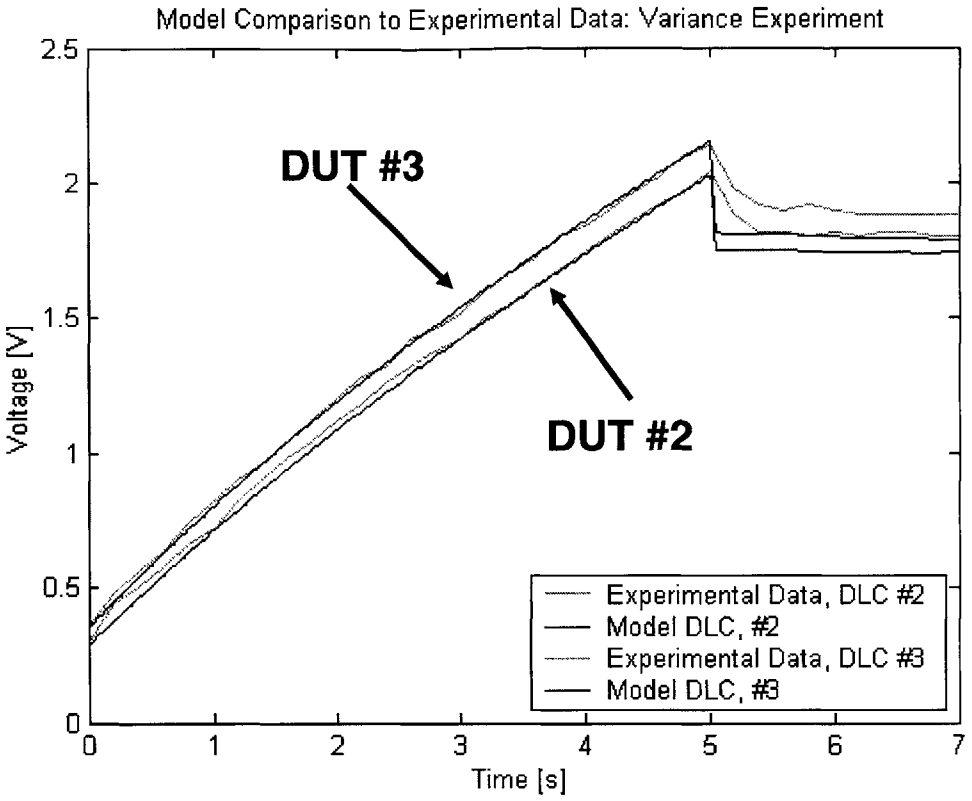

Figure 7.20: Model Comparison to Experimental Data

capacitances of the devices (refer to Fig. 7.21) did show some variation as well, but not on the order of magnitude expected based on the variances given by the manufacture. In charging the devices with a constant current from 0 to ~2.25 V, nearly the full voltage range of this model of device, resulted in all the devices reaching a maximum voltage within 0.1 V of one another (~4% deviation). In conclusion, this experiment has provided evidence that the specified device variances of current state-of-the-art manufactured carbon-based DLCs may be liberally estimated by the manufactures and in fact the actual device variances may be quit low. This batch of tested devices is very small and no hard conclusion to that fact may be drawn, however, no large variances were detected in the batch of test samples. This experiment did not investigate the variation in the devices other capacitance and resistance terms (C_m, C_s, R_m, and R_s), nor did it investigate the variances in leakage resistance (an important consideration when using these devices for long term energy storage).

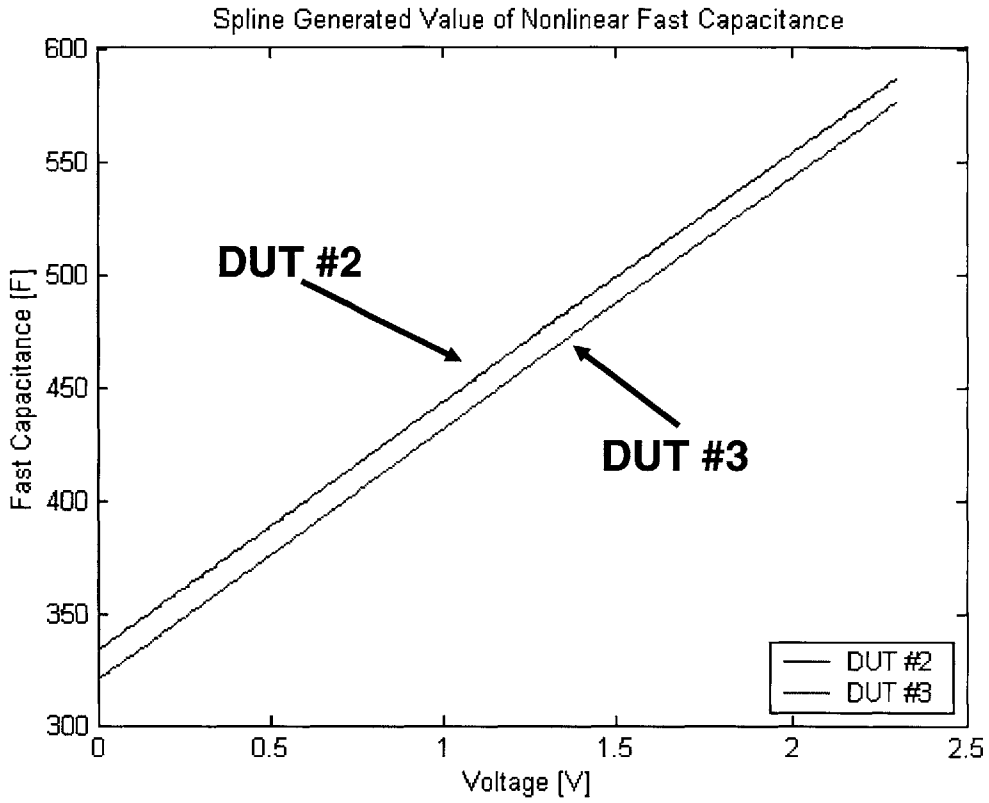

Figure 7.21: Spline Generated Value of Nonlinear Capacitance for DLC #2 & 3

Chapter 8

Conclusions

8.1 Introduction

As with many research projects, the initial plans and focus of the project are modified and changed along the way. This project was no different. The modeling of these devices has long been a goal of this project; however, the task became larger than initially expected once the nonlinearities of these devices were discovered.

The main goals of this work are as follows. 1) To give a basic and comprehensive explanation of some of the many different electrochemical capacitor technologies commercially available or under investigation in research laboratories today. Additionally, this research works to give an introduction/overview of some of the electrochemical phenomenon present in these devices. 2) To produce a simple, yet accurate, modeling procedure to capture the behavior of these double layer capacitors (ones whose primary means of energy storage is through an electrostatic mechanism). This modeling procedure should ideally require no special software other than what is considered a common software package to many electrical engineers today. And, the laboratory measurements required for collecting data points should not be exceedingly laborious or difficult to collect. It is desired that the end user of this developed procedure could follow the steps outlined in this work with little more effort than one would exert to follow a culinary recipe. 3) To validate through a series of experiments the accuracy of the modeling procedure. This series of experiments should attempt to mimic some of the conditions such a device would be subjected to as part of an advanced automotive electrical system (high and low charging currents, delays, etc.). 4) To quantitatively investigate the temperature trends of these device (both high and low temperatures). 5) And finally, to investigate the parameter variances of the devices (most importantly the parameters called C_f and R_f throughout this thesis).

8.2 Evaluation of Thesis Objectives and Contributions

The evaluation of the above mentioned goals of this work will proceed in the order in which they have been listed in the introduction.

This thesis gives an outline of some of the many types of technologies under investigation today for these electrochemical capacitors. The investigation is broken down into the primary constituents of these devices which determines device's the primary behavior, whether it's energy storage via electrochemical reactions or electrostatic mechanisms. The overview includes a discussion of the different types of electrode materials (and in some cases the additional manufacturing components required to construct these electrodes), many of the different electrolytes possible for these systems (aqueous based, organic based, etc.), a discussion of the distributed resistances and capacitances of these devices, and why there is a need for complex mathematical models for the description of these devices.

The modeling procedure presented in this thesis meets these goals. The procedure has been broken down into steps and results in a simple, easy to follow method for determining the model of a given device (assuming the device's primary means of energy storage is electrostatic). The procedure requires common engineering software (Matlab®) and presents the needed Matlab® function required to capture some of the nonlinear characteristics. The laboratory experiments/measurements are relatively simple to perform and do not require the accumulation of large amounts of data. And finally, the accuracy achievable with this method is found to be very good. The results of the model's comparison to the device's performance are extensively presented in Chapter 4 as well as throughout the thesis.

The device's performance with fluctuations in temperature was also a concern as temperature variations are inherent to the environment in which automotive electronics are a part of. The work successfully investigated the trends of the DLC model parameters with temperature variation. A clear trend was seen in many of the parameters (confirming this researchers initial idea of the parameter's trends), however due to the relative change in temperature of the high temperature experiments and the inherent experimental error in the measurements, some parameters fail to show a clear trend. Either way, models were determined for the temperature experiments and a better understanding of the phenomenon gained.

Finally, the work concludes with the investigation of device variances. This experiment began with a concern that many device manufacturers presents manufacturing tolerances in the range of 20 - 30%. As outlined in Chapter 7, this could result in a variety of concerns when these devices are used as part of a larger system. The experiments (using a relatively small sample of devices) did show a variation in device parameters, however, these variances

were not as high as initially expected. This experiment provided information to the effect that the device variances may not be as high (as stated by the manufacturer's tolerances) in many of the devices in production or that the variations, if present, may not be as commonplace as initially assumed.

The collection of work presented in this thesis succeeds in presenting a procedure for modeling these devices and addresses some of the concerns engineers would have when considering these devices as a part of their electrical system (temperature, device variation, available technologies, etc.).

Appendix A

Supplemental Material for Chapter 3: Matlab Code

A.1 File Name: expfit

(Experimental data of multi-time constant device)

t=[Enter Experimental Time Data Here];

v=[Enter Experimental Voltage Data Here];

(Single time constant model)

```
tau=(2600)*2000;
vc=exp(-t/tau);
```

(Plot data)

```
semilogy(t/86400,v,t/86400,vc);
title('Experimental Voltage Decay');
legend('DLC','Single Time Constant');
grid on;
xlabel('Time [day]');
ylabel('Voltage [V]');
```

A.2 File Name: model

```
function [time, volt, vexp]=model(ans);
```

(Experimental data)

vexp=[Enter Experimental Data Here];

(Manipulate data)

```
t=0:1/5:14945/5;
data=ans';
time=data(:,1);
volt=data(:,2);
```

(Display data)

```
plot(t,vexp,'m',time(1:14945),volt(1:14945));
axis([0 3000 0 0.6]);
legend( 'Experimental Data', 'Model', 4);
title('Model Comparison to Experimental Data: Room Temp. (~21C)');
xlabel('Time [s]');
ylabel('Voltage [V]');

figure;

plot(t,vexp,'m',time(1:14945),volt(1:14945)); axis([0 300 0 0.6]);
legend( 'Experimental Data', 'Model', 4);
title('Model Comparison to Experimental Data: Room Temp. (~21C)');
xlabel('Time [s]');
ylabel('Voltage [V]');

figure;

plot(t,vexp,'m',time(1:14945),volt(1:14945));
axis([0 30 0 0.6]);
legend( 'Experimental Data', 'Model', 4);
title('Model Comparison to Experimental Data: Room Temp. (~21C)');
xlabel('Time [s]');
ylabel('Voltage [V]');
```

Appendix B

Supplemental Material for Chapter 4: Labview and PSpice

B.1 Labview

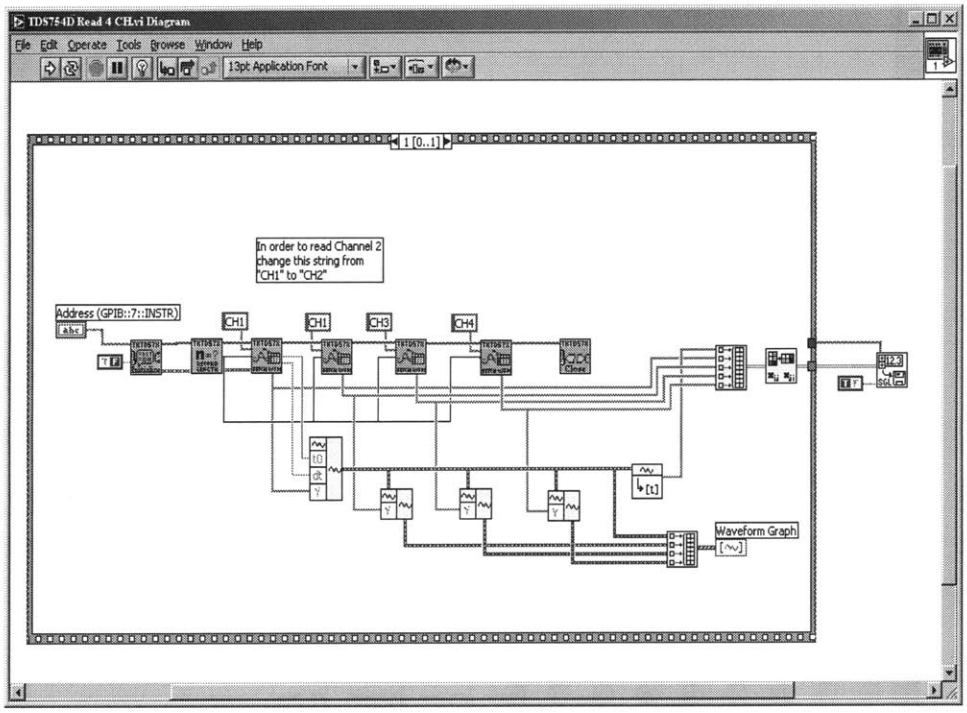

Figure B.1: LabView® Screen Capture

B.2 PSpice

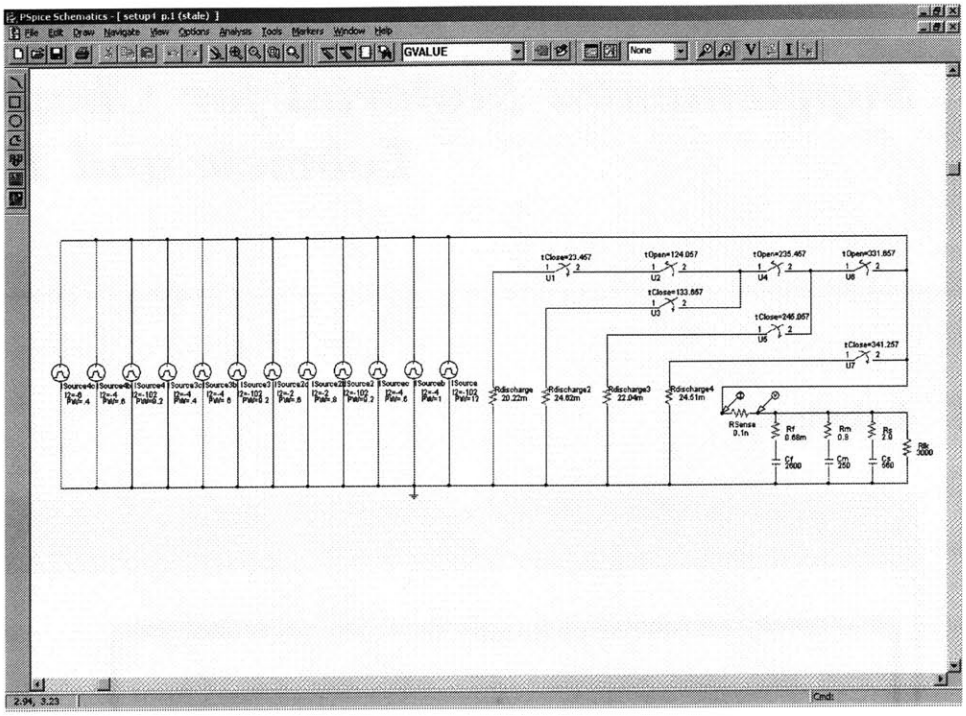

Figure B.2: 100A Simulation Circuit Diagram

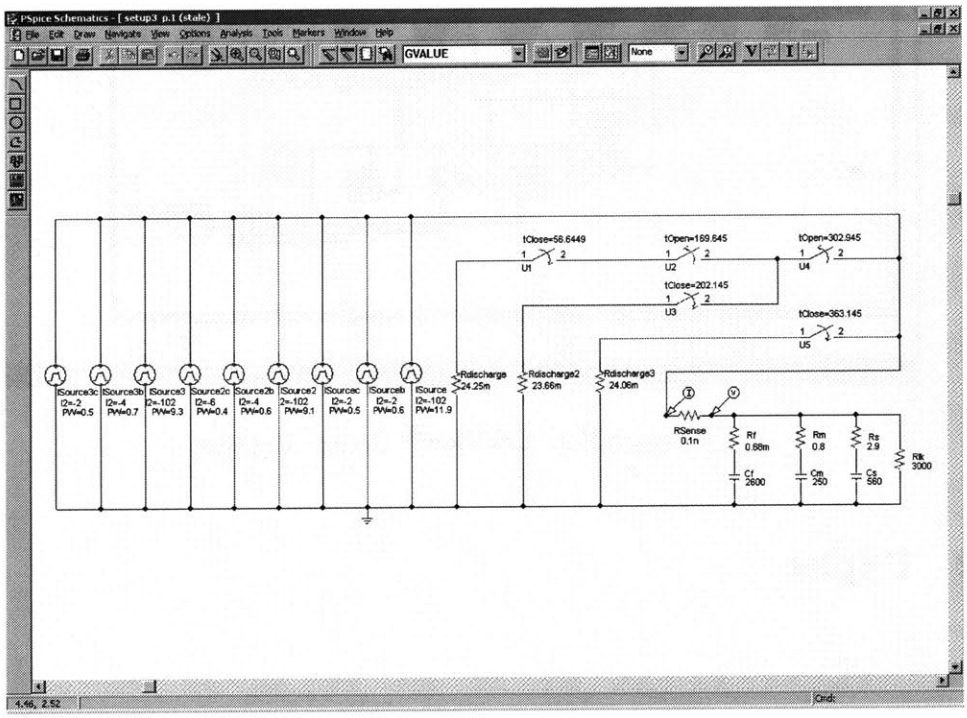

Figure B.3: 100A with Delay Simulation Circuit Diagram

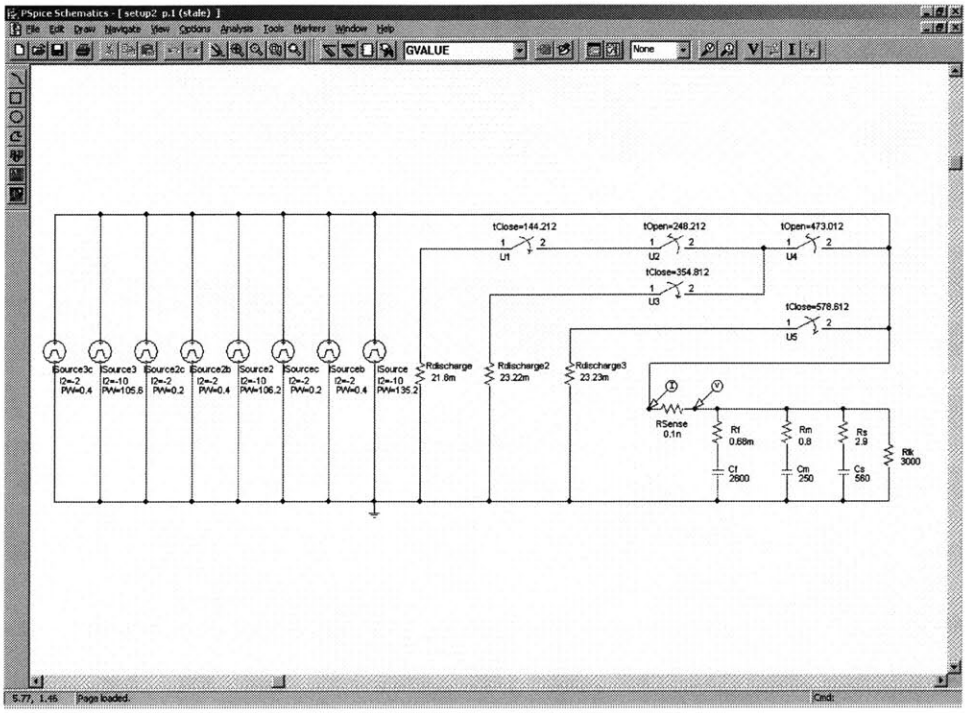

Figure B.4: 10A Simulation Circuit Diagram

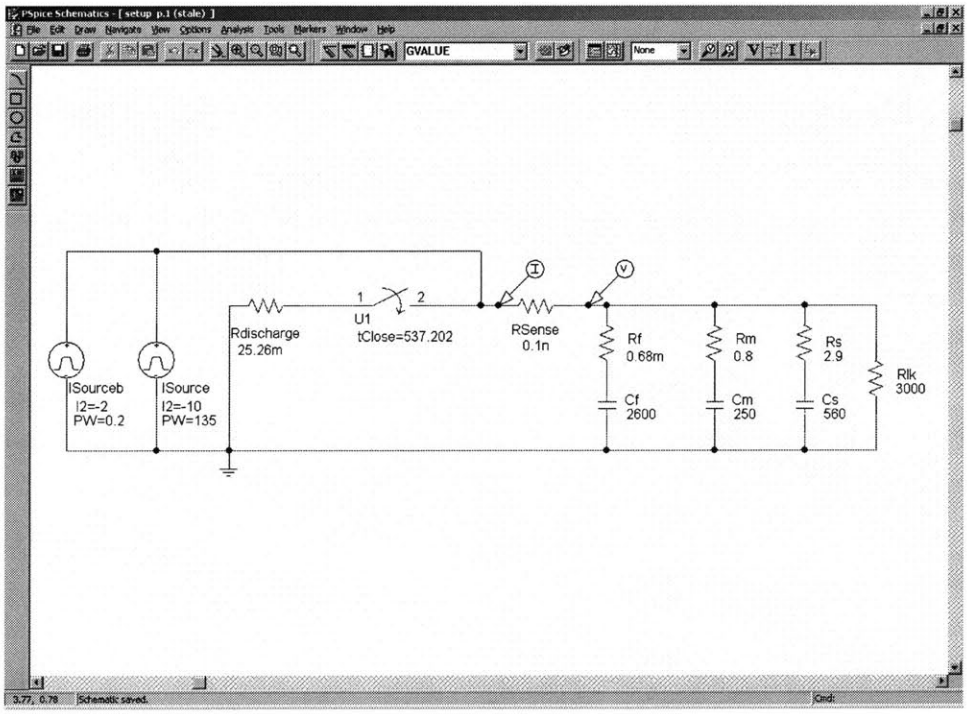

Figure B.5: 10A with Delay Simulation Circuit Diagram

Appendix C

Supplemental Material for Chapter 4: Matlab Code

C.1 File Name: voltagecurrentpower

(Experimental data)

time=[Enter Experimental Data Here];

vcap=[Enter Experimental Data Here];

iprobe=[Enter Experimental Data Here];

power=[Enter Experimental Data Here];

(Display data)

```
subplot(3,1,1) plot(time, vcap);
title('100A Charging With Transition Delay');
ylabel('Voltage [V]');
axis([0 500 0 0.6]);
grid on;

subplot(3,1,2) plot(time, iprobe);
ylabel('Current [A]');
axis([0 500 -25 125]);
grid on;

subplot(3,1,3) plot(time, power);
xlabel('Time [s]');
ylabel('Power [W]');
axis([0 500 -15 60]);
grid on;
```

Appendix D

Supplemental Material for Chapter 5: Matlab Code

D.1 File Name: temp

(Experimental data)

timeHT=[Enter Experimental Data Here];

temperHT=[Enter Experimental Data Here];

timeLT=[Enter Experimental Data Here];

temperLT=[Enter Experimental Data Here];

(Display data)

```
plot(timeHT, temperHT);
title('High Temperature Experiment: Temperature versus Time');
axis([0 300 0 60]);
xlabel('Time [min]');
ylabel('Temperature [degrees C]');

figure;

plot(timeLT, temperLT);
title('Low Temperature Experiment: Temperature versus Time');
axis([0 375 5 -40]);
xlabel('Time [min]');
ylabel('Temperature [degrees C]');
```

D.2 File Name: RT model

```
function [time, volt, vexp]=model(ans);

(Experimental data)

vexp=[ Enter Experimental Data Here ];

(Manipulate data)

t=0:1/5:14945/5;
data=ans';
time=data(:,1);
volt=data(:,2);


(Display data)

plot(t,vexp,'m',time(1:14945),volt(1:14945));
axis([0 3000 0 0.6]);
legend( 'June Experimental Data',4);
legend( 'Experimental Data', 'Model', 4);
title('Model Comparison to Experimental Data: Room Temp. (~21C)');
xlabel('Time [s]');
ylabel('Voltage [V]');


figure;

plot(t,vexp,'m',time(1:14945),volt(1:14945));
axis([0 300 0 0.6]);
legend( 'Experimental Data', 'Model', 4);
title('Model Comparison to Experimental Data: Room Temp. (~21C)');
xlabel('Time [s]');
ylabel('Voltage [V]');


figure;

plot(t,vexp,'m',time(1:14945),volt(1:14945));
axis([0 30 0 0.6]);
legend( 'Experimental Data', 'Model', 4);
title('Model Comparison to Experimental Data: Room Temp. (~21C)');
```

```
xlabel('Time [s]');
ylabel('Voltage [V]');
```

D.3 File Name: HT model

```
function [time, volt, vexp]=model(ans);

(Experimental Data)

vexp=[ Enter Experimental Data Here ];

(Manipulate Data)

t=0:1/5:14945/5;
data=ans';
time=data(:,1);
volt=data(:,2);


(Display data)

plot(t,vexp,'m',time(1:14945),volt(1:14945));
axis([0 3000 0 0.6]);
legend( 'June Experimental Data',4);
legend( 'Experimental Data', 'Model', 4);
title('Model Comparison to Experimental Data: High Temp. (~50C)');
xlabel('Time [s]');
ylabel('Voltage [V]');


figure;

plot(t,vexp,'m',time(1:14945),volt(1:14945));
axis([0 300 0 0.6]);
legend( 'Experimental Data', 'Model', 4);
title('Model Comparison to Experimental Data: High Temp. (~50C)');
xlabel('Time [s]');
ylabel('Voltage [V]');


figure;
```

```
plot(t,vexp,'m',time(1:14945),volt(1:14945));
axis([0 30 0 0.6]);
legend( 'Experimental Data', 'Model', 4);
title('Model Comparison to Experimental Data: High Temp. (~50C)');
xlabel('Time [s]');
ylabel('Voltage [V]');
```

D.4 File Name: LT model

```
function [time, volt, vexp]=model(ans);

(Experimental data)

vexp=[ Enter Experimental Data Here ];

(Manipulate data)

t=0:1/5:14945/5;
data=ans';
time=data(:,1);
volt=data(:,2);


(Display data)

plot(t,vexp,'m',time(1:14945),volt(1:14945));
axis([0 3000 0 0.6]);
legend( 'June Experimental Data',4);
legend( 'Experimental Data', 'Model', 4);
title('Model Comparison to Experimental Data: Low Temp. (~-25C)');
xlabel('Time [s]');
ylabel('Voltage [V]');


figure;

plot(t,vexp,'m',time(1:14945),volt(1:14945));
axis([0 300 0 0.6]);
legend( 'Experimental Data', 'Model', 4);
title('Model Comparison to Experimental Data: Low Temp. (~-25C)');
xlabel('Time [s]');
```

```
ylabel('Voltage [V]');


figure;

plot(t,vexp,'m',time(1:14945),volt(1:14945));
axis([0 30 0 0.6]);
legend( 'Experimental Data', 'Model', 4);
title('Model Comparison to Experimental Data: Low Temp. (~-25C)');
xlabel('Time [s]');
ylabel('Voltage [V]');
```

D.5 File Name: combo

```
(Experimental data RT)

vexp1=[ Enter Experimental Data Here ];

(Experimental data HT)

vexp2=[ Enter Experimental Data Here ];

(Experimental data LT)

vexp3=[ Enter Experimental Data Here ];

(Manipulate data)

t=0:1/5:14945/5;

(Display data)

plot(t,vexp1,'m',t,vexp2, t,vexp3);
axis([0 3000 0 0.6]);
legend( 'Room Temperature', 'High Temperature', 'Low Temperature', 4);
title('DLC Performance with Temperature Variation');
xlabel('Time [s]');
ylabel('Voltage [V]');


figure;
```

```
plot(t,vexp1,'m',t,vexp2, t,vexp3);
axis([0 300 0 0.6]);
legend( 'Room Temperature', 'High Temperature', 'Low Temperature', 4);
title('DLC Performance with Temperature Variation');
xlabel('Time [s]');
ylabel('Voltage [V]');


figure;

plot(t,vexp1,'m',t,vexp2, t,vexp3);
axis([0 30 0 0.6]);
legend( 'Room Temperature', 'High Temperature', 'Low Temperature', 4);
title('DLC Performance with Temperature Variation');
xlabel('Time [s]');
ylabel('Voltage [V]');
```

Appendix E

Supplemental Material for Chapter 6: Matlab Code

E.1 File Name: dave_main

```
clear all;

R2=93.5e-3;
C2=29.03;

h=0.02; (Integration step)
y0=[0; 0; 0]; (Initial conditions–capacitor voltages)
t_span=0 : h : 3000; (Integration span)
[t1,y1]=ode23TB('dave_int',t_span,y0);

(Experimental data)

vexp=[ Enter Experimental Data Here ];

(Time)

t=0:1/5:14945/5;

(Display data)

plot(t,vexp, t_span(1:length(t_span)-1),y1(1:length(y1)-1,2)+R2*C2*diff(y1(:,2))/h,'b');
axis([0 3000 0 3]);
legend( 'Experimental Data', 'Model', 4);
title('Model Comparison to Experimental Data: Nonlinear Experiment');
xlabel('Time [s]');
ylabel('Voltage [V]');

figure;

plot(t,vexp, t_span(1:length(t_span)-1),y1(1:length(y1)-1,2)+R2*C2*diff(y1(:,2))/h,'b');
```

```
axis([0 300 0 3]);
legend( 'Experimental Data', 'Model', 4);
title('Model Comparison to Experimental Data: Nonlinear Experiment');
xlabel('Time [s]');
ylabel('Voltage [V]');

figure;

plot(t,vexp, t_span(1:length(t_span)-1),y1(1:length(y1)-1,2)+R2*C2*diff(y1(:,2))/h,'b');
axis([0 30 0 3]);
legend( 'Experimental Data', 'Model', 4);
title('Model Comparison to Experimental Data: Nonlinear Experiment');
xlabel('Time [s]');
ylabel('Voltage [V]');
```

E.2 File Name: dave_int

```
function v_prime=phase(t,v)

Vtable=[0.76 2.22];
Ctable=[411.8 588.3]; C1=spline(Vtable,Ctable,v(1)); (Interpolating the capacitance from
the table)
R1=1.88e-3;
R2=93.5e-3;
C2=29.03;
R3=4.05;
C3=73.5;
R4=3e3;
Req=1/(1/R1+1/R2+1/R3+1/R4);

Idc=97; (Current source dc current)

v = [-1/(R1*C1)*(1-Req/R1)*v(1)+ 1/(R1*C1)*(Req/R2)*v(2)+ 1/(R1*C1)*(Req/R3)*v(3);...
-1/(R2*C2)*(1-Req/R2)*v(2)+ 1/(R2*C2)*(Req/R1)*v(1)+ 1/(R2*C2)*(Req/R3)*v(3);...
-1/(R3*C3)*(1-Req/R3)*v(3)+ 1/(R3*C3)*(Req/R1)*v(1)+ 1/(R3*C3)*(Req/R2)*v(2)];

exc = Idc* [Req/(R1*C1); Req/(R2*C2); Req/(R3*C3)]*((0.5+0.5*sign(t))-(0.5+0.5*sign(t-
10.6)));

v_prime=v+exc;
```

E.3 File Name: spl

```
Vtable=[0.76 2.22];
Ctable=[411.8 588.3];

v=0:0.01:2.3;

C1=spline(Vtable,Ctable,v);

plot(v,C1);
title('Spline Generated Value of Nonlinear Fast Capacitance');
xlabel('Voltage [V]');
ylabel('Fast Capacitance [F]');
```

Appendix F

Supplemental Material for Chapter 7: Matlab Code

F.1 File Name: modeDUT2

```
clear all;

R2=85.12e-3;
C2=37.5;

h=0.02; (Integration step)
y0=[0; 0; 0]; (Initial conditions–capacitor voltages)
t_span=0 : h : 10; (Integration span)
[t1,y1]=ode23TB('dave_int2',t_span,y0);

(Experimental data)

vexp=[ Enter Experimental Data Here ];

(Time)

t=0:1/5:14927/5;

(Display data)

plot(t,vexp, t_span(1:length(t_span)-1),y1(1:length(y1)-1,2)+R2*C2*diff(y1(:,2))/h,'b');
axis([0 7 0 2.5]);
legend( 'Experimental Data, DLC #2', 'Model, DLC #2', 4);
title('Model Comparison to Experimental Data: Variance Experiment');
xlabel('Time [s]');
ylabel('Voltage [V]');
```

F.2 File Name: dave_int2

```
function v_prime=phase(t,v)

Vtable=[0.82 1.88];
Ctable=[423.8 540.4];

C1=spline(Vtable,Ctable,v(1)); (Interpolating the capacitance from the table)
R1=1.8e-3;
R2=85.12e-3;
C2=37.5;
R3=3.071;
C3=71.53;
R4=3e3;
Req=1/(1/R1+1/R2+1/R3+1/R4);

Idc=160; (Current source dc current)

v = [-1/(R1*C1)*(1-Req/R1)*v(1)+ 1/(R1*C1)*(Req/R2)*v(2)+ 1/(R1*C1)*(Req/R3)*v(3);...
-1/(R2*C2)*(1-Req/R2)*v(2)+ 1/(R2*C2)*(Req/R1)*v(1)+ 1/(R2*C2)*(Req/R3)*v(3);...
-1/(R3*C3)*(1-Req/R3)*v(3)+ 1/(R3*C3)*(Req/R1)*v(1)+ 1/(R3*C3)*(Req/R2)*v(2)];

exc = Idc* [Req/(R1*C1); Req/(R2*C2); Req/(R3*C3)]*((0.5+0.5*sign(t))-(0.5+0.5*sign(t-
5.04)));

v_prime=v+exc;
```

F.3 File Name: File Name: modeDUT3

```
clear all;

R2=71.06e-3;
C2=35.75;

h=0.02; (Integration step)
y0=[0; 0; 0]; (Initial conditions–capacitor voltages)
t_span=0 : h : 10; (Integration span)
[t1,y1]=ode23TB('dave_int3',t_span,y0);

(Experimental data)
```

```
vexp=[ Enter Experimental Data Here ];

(Time)

t=0:1/5:14927/5;

plot(t,vexp, t_span(1:length(t_span)-1),y1(1:length(y1)-1,2)+R2*C2*diff(y1(:,2))/h,'b');
axis([0 7 0 2.5]);
legend( 'Experimental Data, DLC #3', 'Model, DLC #3', 4);
title('Model Comparison to Experimental Data: Variance Experiment');
xlabel('Time [s]');
ylabel('Voltage [V]');
```

F.4 File Name: dave_int3

```
function v_prime=phase(t,v)

Vtable=[0.84 1.98];
Ctable=[413.7 540.4];

C1=spline(Vtable,Ctable,v(1)); R1=2.08e-3;
R2=71.06e-3;
C2=35.75;
R3=4.05;
C3=73.5;
R4=3e3; Req=1/(1/R1+1/R2+1/R3+1/R4);

Idc=160;

v = [-1/(R1*C1)*(1-Req/R1)*v(1)+ 1/(R1*C1)*(Req/R2)*v(2)+ 1/(R1*C1)*(Req/R3)*v(3);...
-1/(R2*C2)*(1-Req/R2)*v(2)+ 1/(R2*C2)*(Req/R1)*v(1)+ 1/(R2*C2)*(Req/R3)*v(3);...
-1/(R3*C3)*(1-Req/R3)*v(3)+ 1/(R3*C3)*(Req/R1)*v(1)+ 1/(R3*C3)*(Req/R2)*v(2)];

exc = Idc* [Req/(R1*C1); Req/(R2*C2); Req/(R3*C3)]*((0.5+0.5*sign(t))-(0.5+0.5*sign(t-
5.04)));

v_prime=v+exc;
```

F.5 File Name: File Name: modeDUTcombo

```
clear all;

(DUT _2)

R2a=85.12e-3;
C2a=37.5;

(DUT#3)

R2b=93.5e-3;
C2b=29.03;

h=0.02; (Integration step)
y0=[0; 0; 0]; (Initial conditions–capacitor voltages)
t_span=0 :h :10; (Integration span)
[t1,y1]=ode23TB('dave_int2',t_span,y0);
[t2,y2]=ode23TB('dave_int3',t_span,y0);


(Experimental data DUT #2)

vexp2=[ Enter Experimental Data Here ];

(Experimental Data DUT #3)

vexp3=[ Enter Experimental Data Here ];

t=0:1/5:14927/5;

plot(t,vexp2, t_span(1:length(t_span)-1),y1(1:length(y1)-1,2)+R2a*C2a*diff(y1(:,2))/h,'b', t,vexp3,
t_span(1:length(t_span)-1),y2(1:length(y2)-1,2)+R2b*C2b*diff(y2(:,2))/h,'r');
axis([0 7 0 2.5]);
legend('Experimental Data, DLC _2', 'Model DLC, _2', 'Experimental Data, DLC _3',
'Model DLC, _3', 4);
title('Model Comparison to Experimental Data: Variance Experiment');
xlabel('Time [s]');
ylabel('Voltage [V]');
```

F.6 File Name: spl

```
(DUT #2)

Vtable=[0.82 1.88];
Ctable=[423.8 540.4];

(DUT #3)

Vtable2=[0.84 1.98];
Ctable2=[413.7 540.4];

(Voltage range)

v=0:0.01:2.3;

(Interpolating the capacitance from the table)

C1=spline(Vtable,Ctable,v);
C2=spline(Vtable2,Ctable2,v);

plot(v,C1,v,C2);
title('Spline Generated Value of Nonlinear Fast Capacitance');
xlabel('Voltage [V]'); ylabel('Fast Capacitance [F]');
legend('DUT #2', 'DUT #3', 4);
```

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